V_{DSM}	=	5200 V
I_{TAVM}	=	1975 A
I_{TRMS}	=	3100 A
I_{TSM}	=	29000 A
V_{T0}	=	1.02 V
r_T	=	0.320 mW

Phase Control Thyristor

5STP 17H5200

Doc. No. 5SYA1049-02 Aug.00

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**

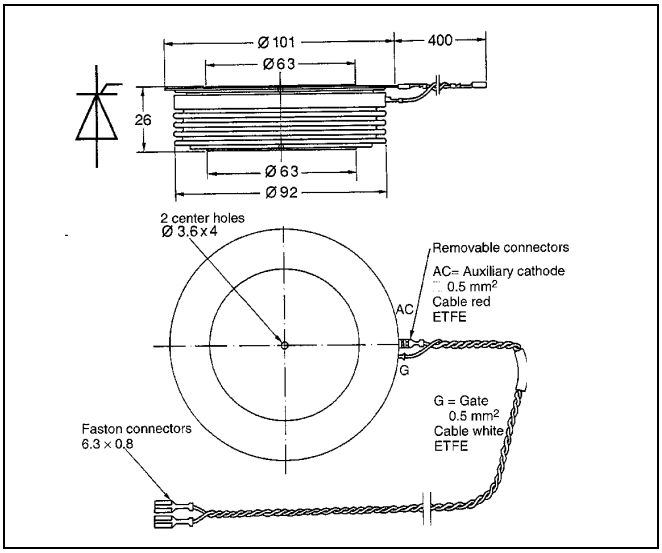
Blocking

Part Number	**5STP 17H5200**	**5STP 17H5000**	**5STP 17H4600**	Conditions
V_{DSM} V_{RSM}	5200 V	5000 V	4600 V	f = 5 Hz, t_p = 10ms
V_{DRM} V_{RRM}	4400 V	4200 V	4000 V	f = 50 Hz, t_p = 10ms
V_{RSM1}	5700 V	5500 V	5100 V	t_p = 5 ms, single pulse
I_{DSM}	≤ 400 mA			V_{DSM}
I_{RSM}	≤ 400 mA			V_{RSM}
dV/dt_{crit}	2000 V/µs		@ Exp. to 0.67xV_{DRM}	T_j = 125°C

V_{DRM}/ V_{RRM} are equal to V_{DSM}/ V_{RSM} values up to T_j = 110°C

Mechanical data

F_M	Mounting force	nom.	50	kN
		min.	45	kN
		max.	60	kN
a	Acceleration			
	Device unclamped		50	m/s^2
	Device clamped		100	m/s^2
m	Weight		0.9	kg
D_S	Surface creepage distance		36	mm
D_a	Air strike distance		15	mm



On-state

I_{TAVM}	Max. average on-state current	1975 A	Half sine wave, T_C = 70°C		
I_{TRMS}	Max. RMS on-state current	3100 A			
I_{TSM}	Max. peak non-repetitive surge current	29000 A	tp = 10 ms	T_j = 125°C	
		31000 A	tp = 8.3 ms	After surge:	
I^2t	Limiting load integral	4205 kA^2s	tp = 10 ms	$V_D = V_R$ = 0V	
		3990 kA^2s	tp = 8.3 ms		
V_T	On-state voltage	1.68 V	I_T = 2000 A		
V_{T0}	Threshold voltage	1.02 V	I_T = 1000 - 3000 A	T_j = 125°C	
r_T	Slope resistance	0.320 mΩ			
I_H	Holding current	30-80 mA	T_j = 25°C		
		15-60 mA	T_j = 125°C		
I_L	Latching current	150-600 mA	T_j = 25°C		
		50-200 mA	T_j = 125°C		

Switching

di/dt_{crit}	Critical rate of rise of on-state current	100 A/µs	Cont.	$V_D \le 0.67 \cdot V_{DRM}$ T_j = 125°C	
		200 A/µs	60 sec.	I_{TRM} = 3000 A f = 50 Hz	
				I_{FG} = 2.0 A t_r = 0.5 µs	
t_d	Delay time	≤ 3.0 µs	$V_D = 0.4 \cdot V_{DRM}$	I_{FG} = 2.0 A t_r = 0.5 µs	
t_q	Turn-off time	≤ 700 µs	$V_D \le 0.67 \cdot V_{DRM}$	I_{TRM} = 3000 A T_j = 125°C	
			dv_D/dt = 20V/µs	V_R > 200 V	
Q_{rr}	Recovery charge min	4800 µAs		di_T/dt = -5 A/µs	
	max	6200 µAs			

Triggering

V_{GT}	Gate trigger voltage	2.6 V	T_j = 25°C
I_{GT}	Gate trigger current	400 mA	T_j = 25°C
V_{GD}	Gate non-trigger voltage	0.3 V	$V_D = 0.4 \cdot V_{DRM}$
I_{GD}	Gate non-trigger current	10 mA	$V_D = 0.4 \cdot V_{DRM}$
V_{FGM}	Peak forward gate voltage	12 V	
I_{FGM}	Peak forward gate current	10 A	
V_{RGM}	Peak reverse gate voltage	10 V	
P_G	Maximum gate power loss	3 W	

Thermal

$T_{j\,max}$	Max. junction temperature	125°C	
$T_{j\,stg}$	Storage temperature range	-40...150°C	
R_{thJC}	Thermal resistance junction to case	20 K/kW	Anode side cooled
		20 K/kW	Cathode side cooled
		10 K/kW	Double side cooled
R_{thCH}	Thermal resistance case to heat sink	4 K/kW	Single side cooled
		2 K/kW	Double side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/t_i})$$

i	1	2	3	4
R_i(K/kW)	6.52	1.55	1.67	0.49
τ_i(s)	0.4562	0.0792	0.0088	0.0037

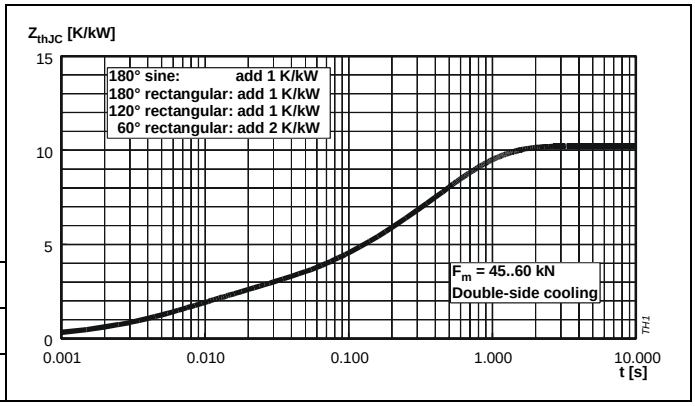


Fig. 1 Transient thermal impedance junction to case.

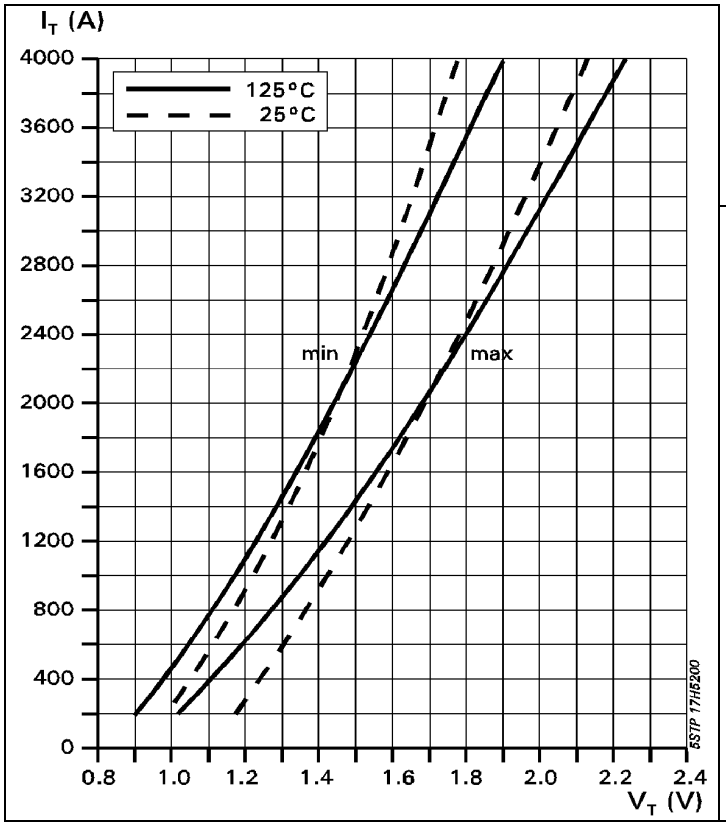


Fig 2. On-state characteristics.

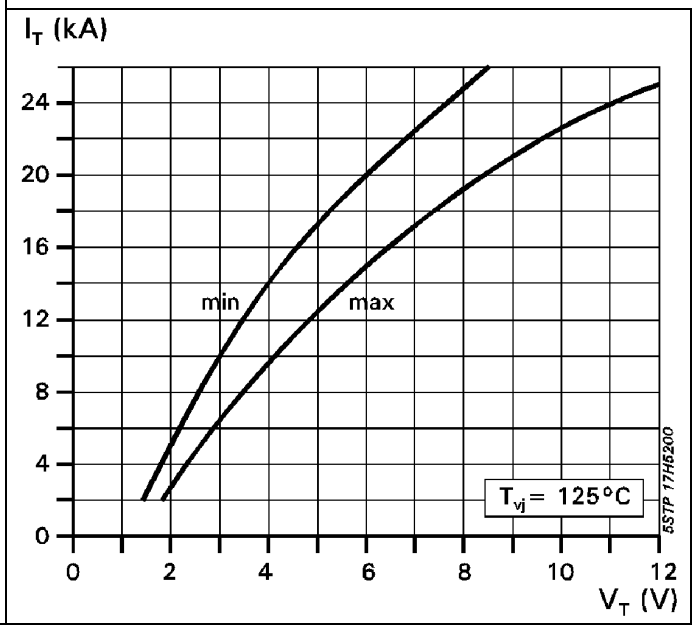


Fig. 3 On state characteristics.

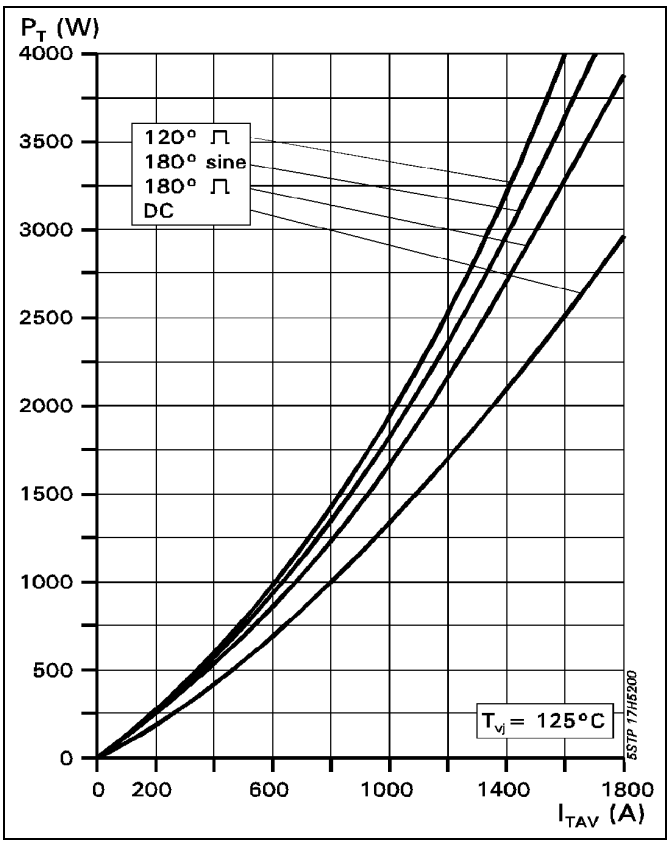


Fig. 4 On-state power dissipation vs. mean on-state current. Turn-on losses excluded.

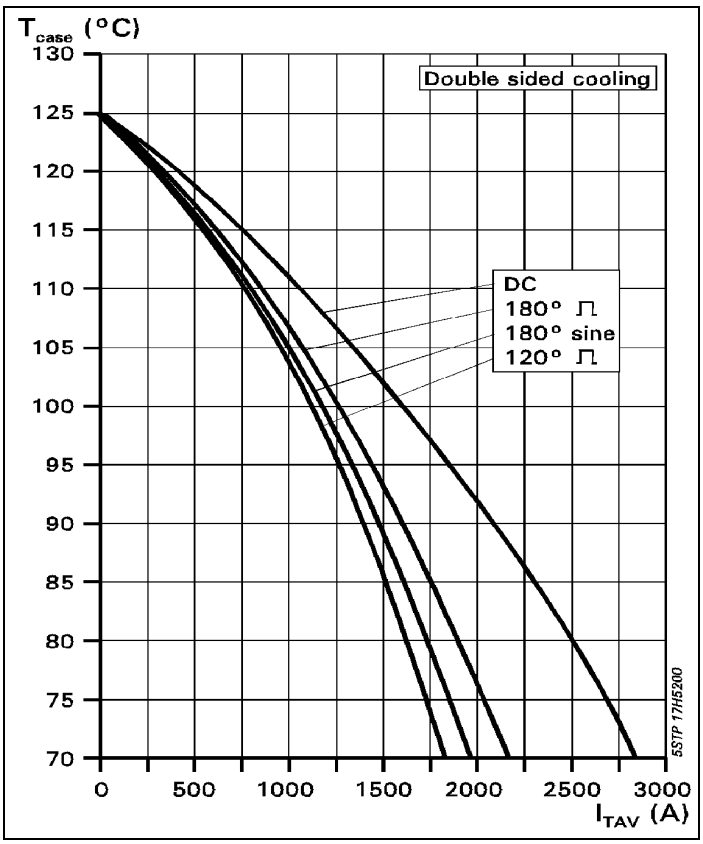


Fig. 5 Max. permissible case temperature vs. mean on-state current.

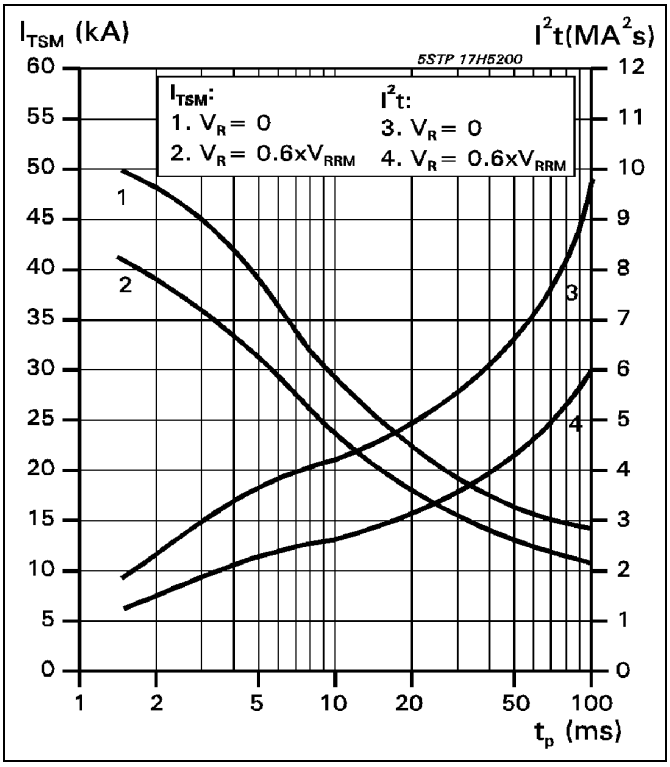


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

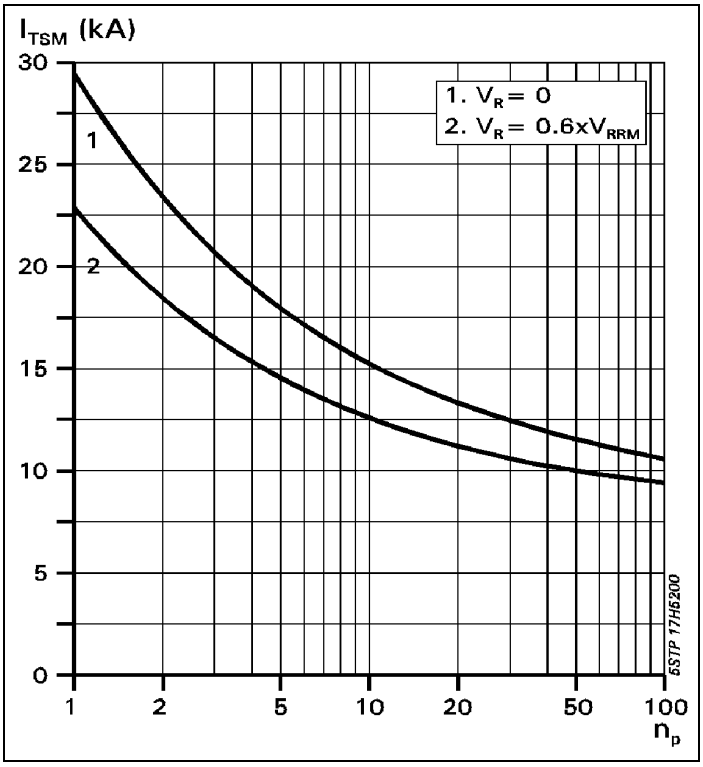


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

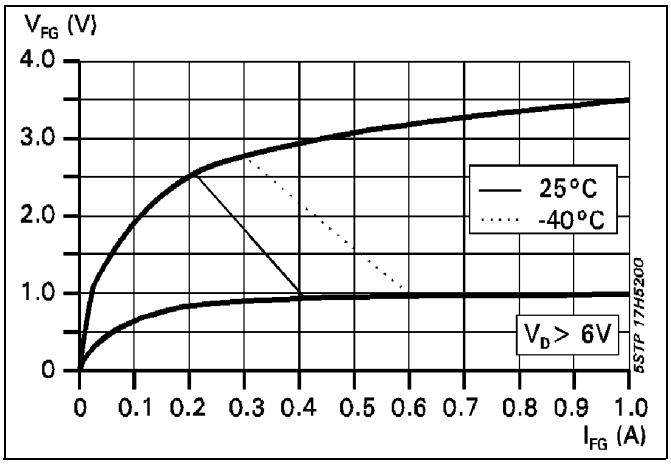


Fig. 8 Gate trigger characteristics.

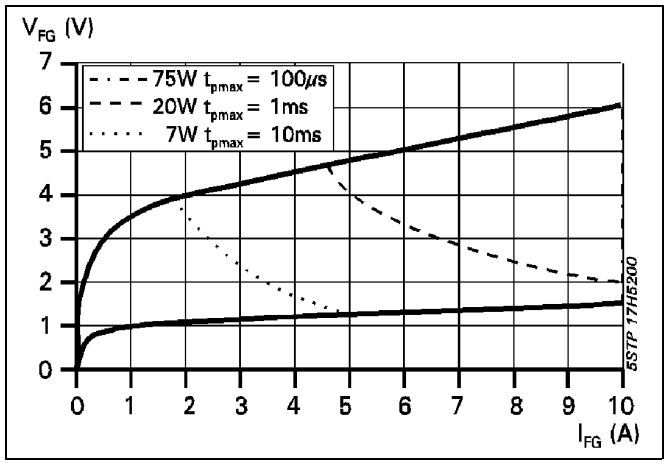


Fig. 9 Max. peak gate power loss.

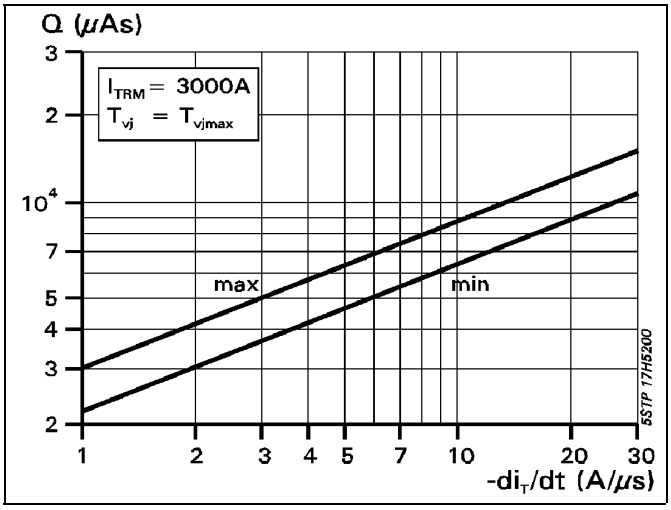


Fig. 10 Recovery charge vs. decay rate of on-state current.

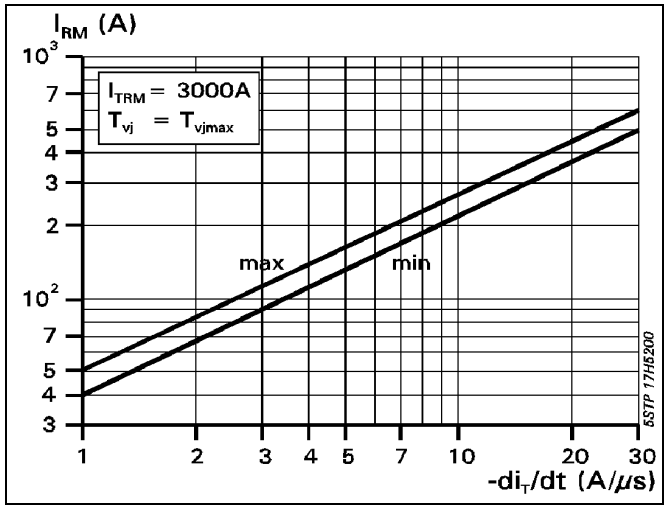


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

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