

V_{DSM}	=	5200 V
I_{TAVM}	=	3875 A
I_{TRMS}	=	6090 A
I_{TSM}	=	55000 A
V_{T0}	=	1.03 V
r_T	=	0.160 mW

Phase Control Thyristor

5STP 34Q5200

Doc. No. 5SYA1052-01 Sep.00

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate.

Blocking

Part Number	5STP 34Q5200	5STP 34Q5000	5STP 34Q4600	Conditions
V_{DSM} V_{RSM}	5200 V	5000 V	4600 V	$f = 5$ Hz, $t_p = 10$ ms
V_{DRM} V_{RRM}	4400 V	4200 V	4000 V	$f = 50$ Hz, $t_p = 10$ ms
V_{RSM1}	5700 V	5500 V	5100 V	$t_p = 5$ ms, single pulse
I_{DSM}	≤ 500 mA			V_{DSM}
I_{RSM}	≤ 500 mA			V_{RSM}
dV/dt_{crit}	2000 V/ μ s			@ Exp. to $0.67 \times V_{DRM}$
$T_j = 125^\circ\text{C}$				

V_{DRM}/V_{RRM} are equal to V_{DSM}/V_{RSM} values up to $T_j = 110^\circ\text{C}$

Mechanical data

F_M	Mounting force	nom.	90 kN
		min.	81 kN
		max.	108 kN
a	Acceleration		
	Device unclamped		50 m/s ²
	Device clamped		100 m/s ²
m	Weight		2.1 kg
D_S	Surface creepage distance		36 mm
D_a	Air strike distance		15 mm

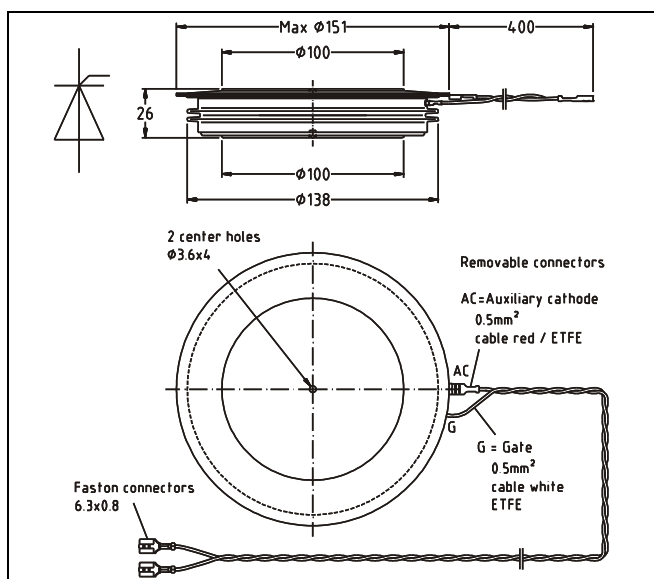


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On-state

I_{TAVM}	Max. average on-state current	3875 A	Half sine wave, $T_C = 70^\circ\text{C}$	
I_{TRMS}	Max. RMS on-state current	6090 A		
I_{TSM}	Max. peak non-repetitive surge current	55000 A	$t_p = 10 \text{ ms}$	$T_j = 125^\circ\text{C}$ After surge: $V_D = V_R = 0\text{V}$
		60000 A	$t_p = 8.3 \text{ ms}$	
I^2t	Limiting load integral	15125 kA^2s	$t_p = 10 \text{ ms}$	
		14940 kA^2s	$t_p = 8.3 \text{ ms}$	
V_T	On-state voltage	1.54 V	$I_T = 3000 \text{ A}$	$T_j = 125^\circ\text{C}$
V_{T0}	Threshold voltage	1.03 V	$I_T = 2300 - 7000 \text{ A}$	
r_T	Slope resistance	0.160 $\text{m}\Omega$		
I_H	Holding current	50-125 mA	$T_j = 25^\circ\text{C}$	
		20-75 mA	$T_j = 125^\circ\text{C}$	
I_L	Latching current	100-500 mA	$T_j = 25^\circ\text{C}$	
		75-250 mA	$T_j = 125^\circ\text{C}$	

Switching

di/dt_{crit}	Critical rate of rise of on-state current	250 $\text{A}/\mu\text{s}$	Cont.	$V_D \leq 0.67 \cdot V_{DRM}$ $T_j = 125^\circ\text{C}$ $I_{TRM} = 3000 \text{ A}$ $f = 50 \text{ Hz}$ $I_{FG} = 2.0 \text{ A}$ $t_r = 0.5 \mu\text{s}$
		500 $\text{A}/\mu\text{s}$	60 sec.	
t_d	Delay time	$\leq 3.0 \mu\text{s}$	$V_D = 0.4 \cdot V_{DRM}$	$I_{FG} = 2.0 \text{ A}$ $t_r = 0.5 \mu\text{s}$
t_q	Turn-off time	$\leq 700 \mu\text{s}$	$V_D \leq 0.67 \cdot V_{DRM}$ $dv_D/dt = 20\text{V}/\mu\text{s}$	$I_{TRM} = 3000 \text{ A}$ $T_j = 125^\circ\text{C}$ $V_R > 200 \text{ V}$
Q_{rr}	Recovery charge	min	7000 μAs	$di_T/dt = -5 \text{ A}/\mu\text{s}$
		max	9000 μAs	

Triggering

V_{GT}	Gate trigger voltage	2.6 V	$T_j = 25^\circ\text{C}$
I_{GT}	Gate trigger current	400 mA	$T_j = 25^\circ\text{C}$
V_{GD}	Gate non-trigger voltage	0.3 V	$V_D = 0.4 \cdot V_{DRM}$
I_{GD}	Gate non-trigger current	10 mA	$V_D = 0.4 \cdot V_{DRM}$
V_{FGM}	Peak forward gate voltage	12 V	
I_{FGM}	Peak forward gate current	10 A	
V_{RGM}	Peak reverse gate voltage	10 V	
P_G	Maximum gate power loss	3 W	

Thermal

$T_{j\ max}$	Max. junction temperature	125°C	
$T_{j\ stg}$	Storage temperature range	-40...150°C	
R_{thJC}	Thermal resistance junction to case	10 K/kW	Anode side cooled
		10 K/kW	Cathode side cooled
		5 K/kW	Double side cooled
R_{thCH}	Thermal resistance case to heat sink	2 K/kW	Single side cooled
		1 K/kW	Double side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i (K/kW)	3.27	0.736	0.661	0.312
τ_i (s)	0.5237	0.1082	0.02	0.0075

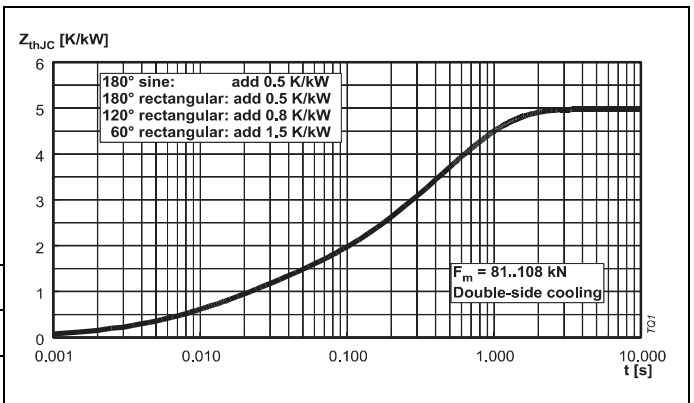


Fig. 1 Transient thermal impedance junction to case.

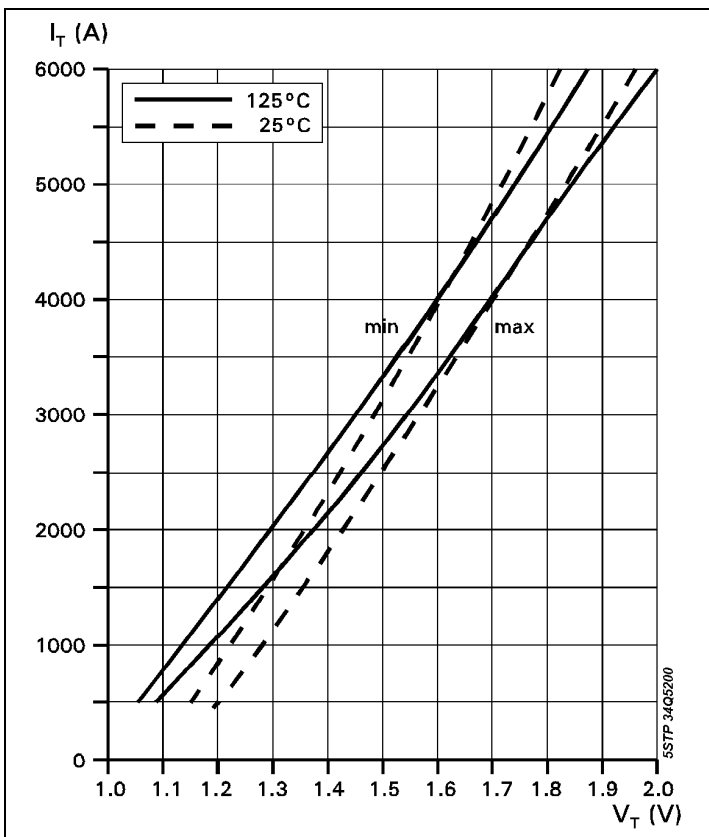


Fig 2. On-state characteristics.

On-state characteristic model:

$$V_T = A + B \cdot i_T + C \cdot \ln(i_T + 1) + D \cdot \sqrt{i_T}$$

Valid for $i_T = 500 - 14000$ A

A	B	C	D
1.0649	0.000105	-0.038879	0.008155

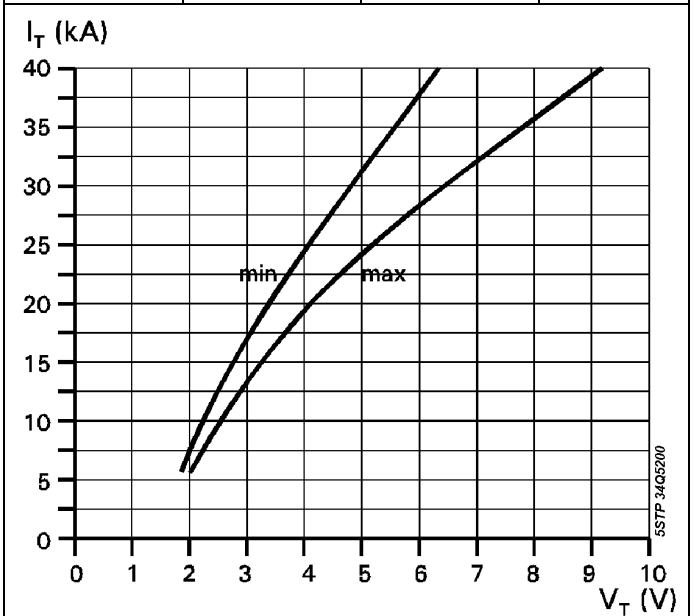


Fig. 3 On state characteristics.

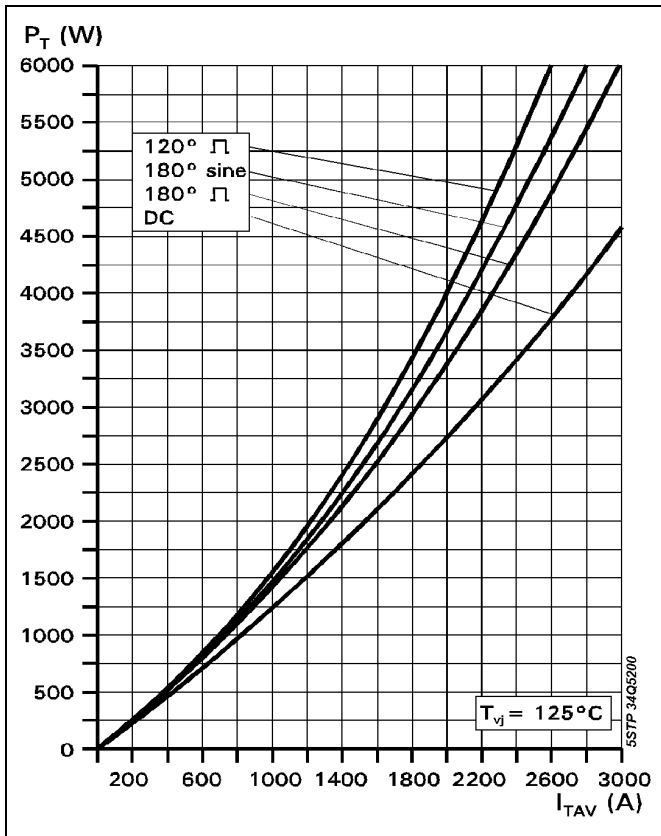


Fig. 4 On-state power dissipation vs. mean on-state current. Turn-on losses excluded.

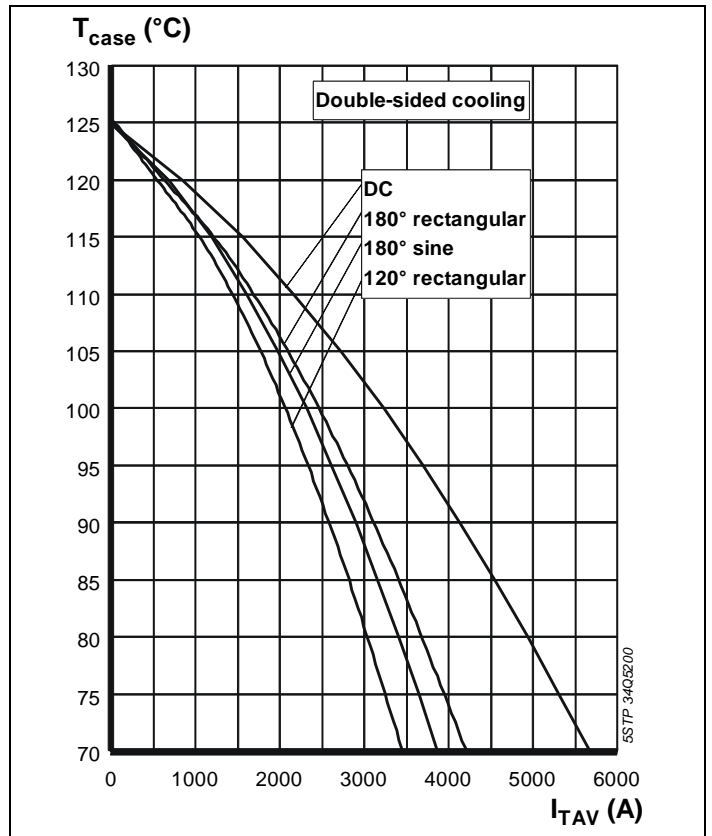


Fig. 5 Max. permissible case temperature vs. mean on-state current.

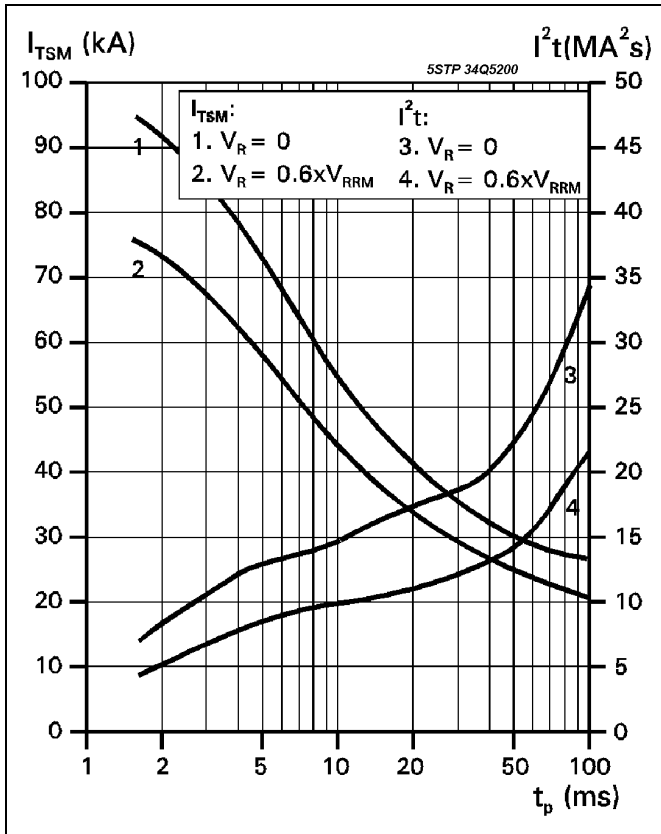


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

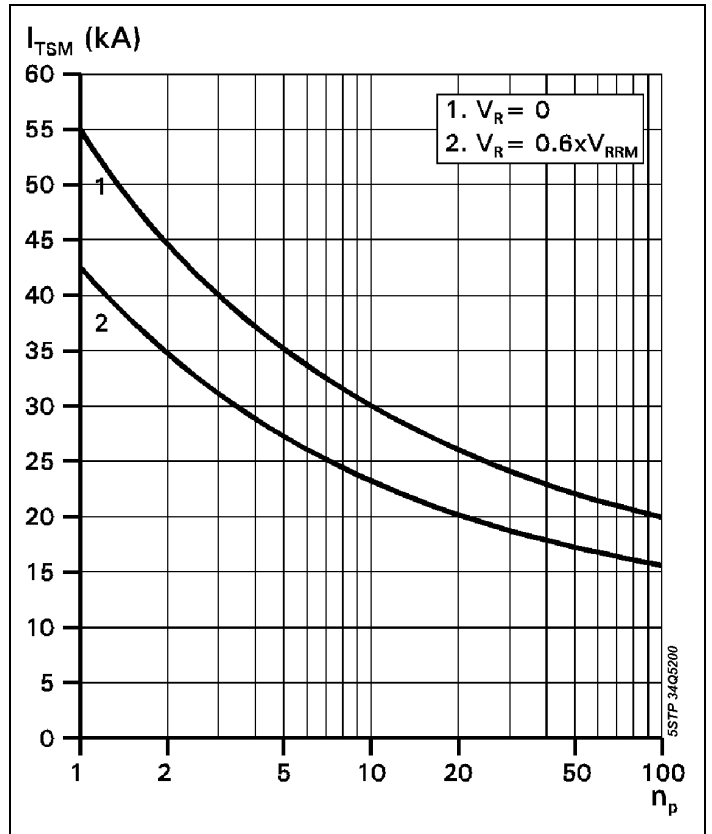


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

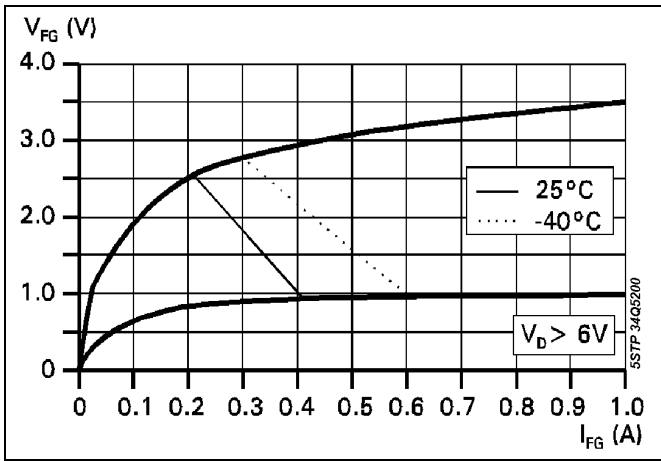


Fig. 8 Gate trigger characteristics.

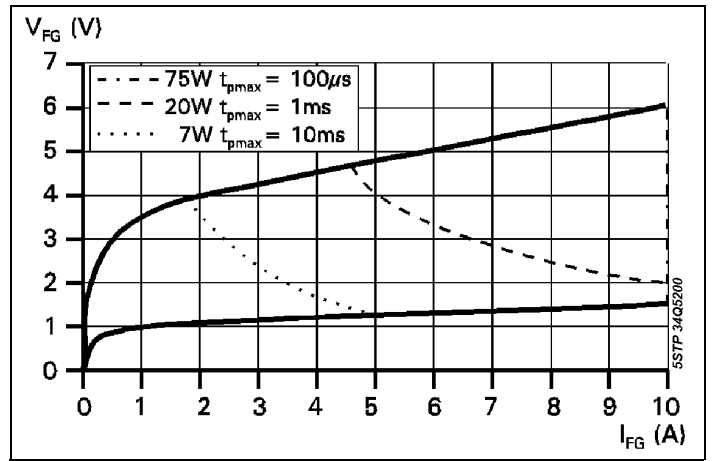


Fig. 9 Max. peak gate power loss.

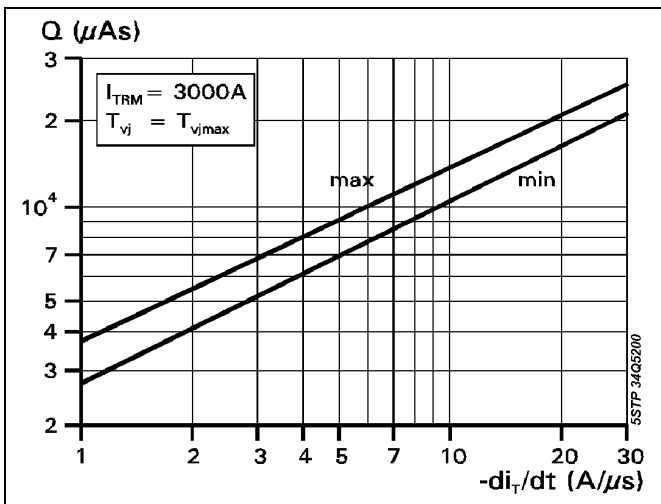


Fig. 10 Recovery charge vs. decay rate of on-state current.

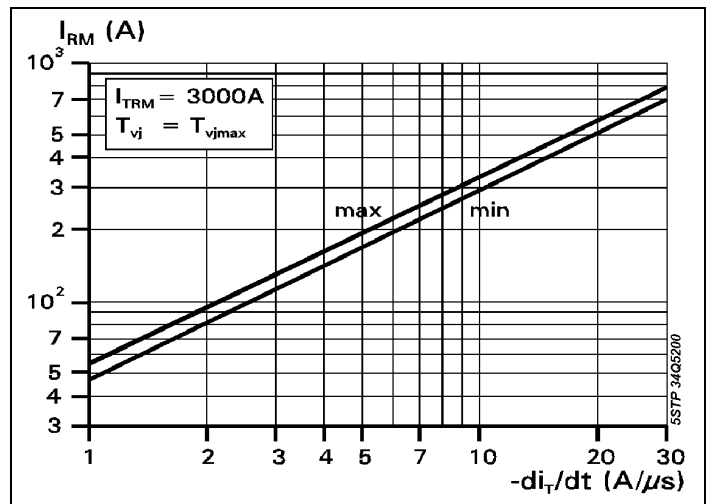


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

Turn –off time, typical parameter relationship.

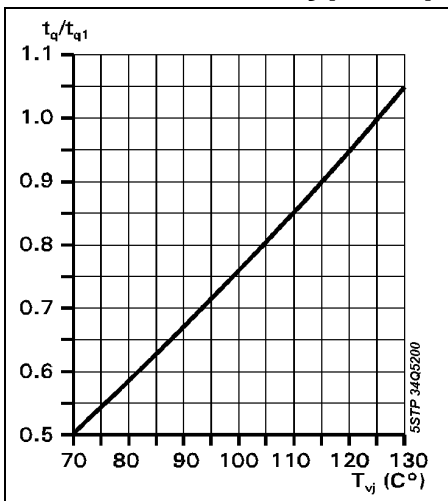


Fig. 12 $t_q/t_{q1} = f_1(T_j)$

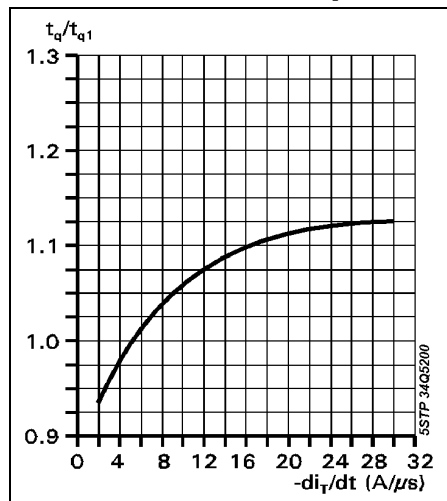


Fig. 13 $t_q/t_{q1} = f_2(-di/dt)$

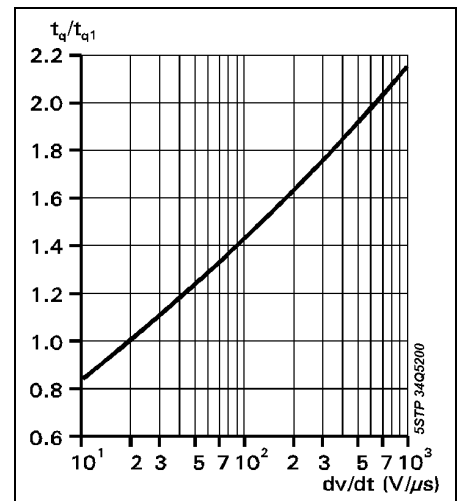


Fig. 14 $t_q/t_{q1} = f_3(dv/dt)$

$t_q = t_{q1} \cdot t_q/t_{q1} f_1(T_j) \cdot t_q/t_{q1} f_2(-di/dt) \cdot t_q/t_{q1} f_3(dv/dt)$
 t_{q1} : at normalized values (see page 2)
 t_q : at varying conditions

Turn-on and Turn-off losses

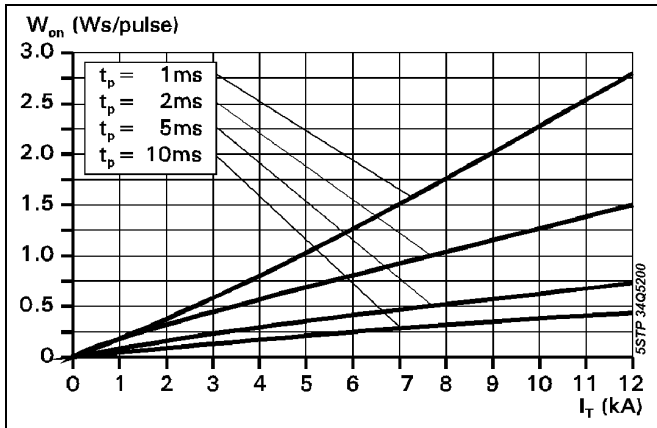


Fig. 15 $W_{on} = f(I_T, t_p)$, $T_j = 125^\circ\text{C}$.
Half sinusoidal waves.

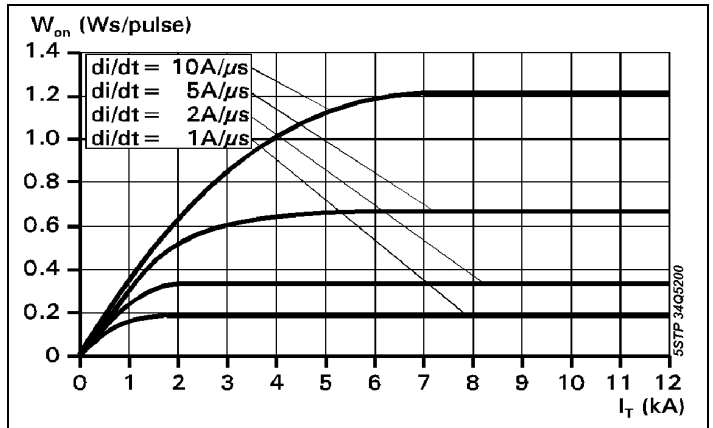


Fig. 16 $W_{on} = f(I_T, di/dt)$, $T_j = 125^\circ\text{C}$.
Rectangular waves.

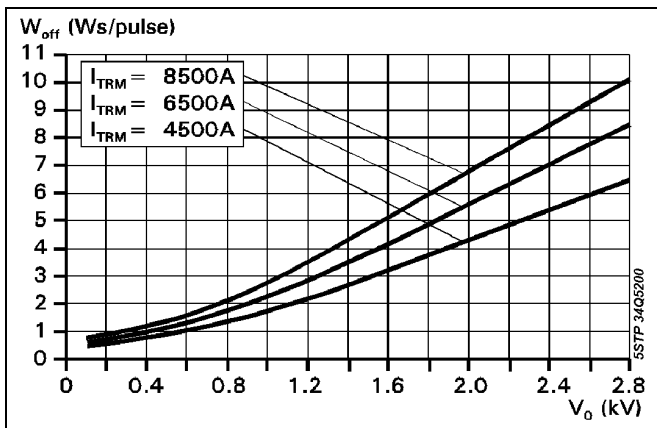


Fig. 17 $W_{off} = f(V_o, I_T)$, $T_j = 125^\circ\text{C}$.
Half sinusoidal waves. $t_p = 10$ ms.

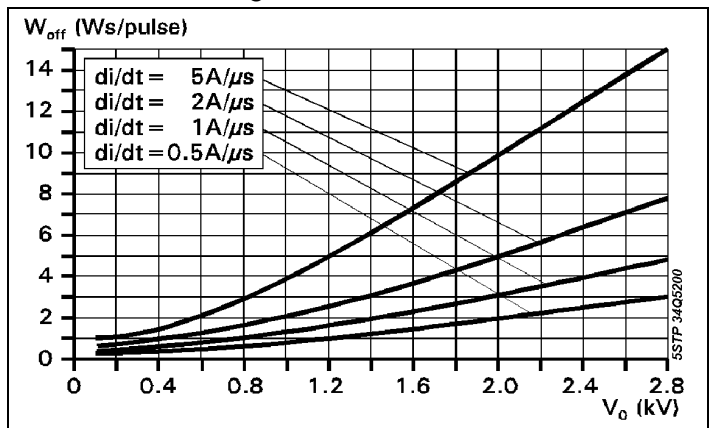


Fig. 18 $W_{off} = f(V_o, di/dt)$, $T_j = 125^\circ\text{C}$.
Rectangular waves.

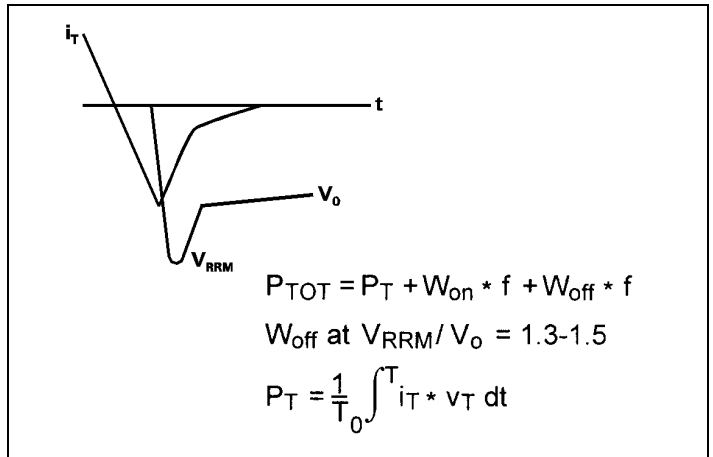


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