





# **Phase Control Thyristor**

**Preliminary Information** 

DS5940-1.0 March 2009 (LN 26623)

#### **FEATURES**

- Double Side Cooling
- High Surge Capability

#### **APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

#### **VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages V <sub>DRM</sub> and V <sub>RRM</sub> V	Conditions
DCR3990A52* DCR3990A50 DCR3990A45	5200 5000 4500	$\begin{split} T_{vj} &= \text{-}40^\circ\!\text{C to }125^\circ\!\text{C},\\ I_{DRM} &= I_{IRRM} = 300\text{mA},\\ V_{DRM}, V_{RRM}t_p &= 10\text{ms},\\ V_{DSM}\&V_{RSM} &= \\ V_{DRM}\&V_{RRM} + 100V\\ respectively \end{split}$

Lower voltage grades available. \*5000V @ -40°C, 5200V @ 0°C

### **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

#### DCR3990A52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### **KEY PARAMETERS**

$V_{DRM}$	5200V
$I_{T(AV)}$	3990A
I <sub>TSM</sub>	53400A
dV/dt*	2000V/μs
dl/dt	400Α/μs
	•

\* Higher dV/dt selections available

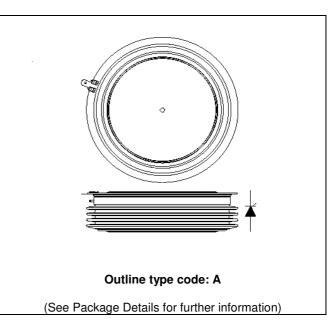


Fig. 1 Package outline





## **CURRENT RATINGS**

## $T_{\text{case}}$ = 60 °C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Si	de Cooled			
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	3990	Α
I <sub>T(RMS)</sub>	RMS value	-	6270	Α
I <sub>T</sub>	Continuous (direct) on-state current	-	5640	Α

## **SURGE RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine, T <sub>case</sub> = 125 ℃	53.4	kA
l <sup>2</sup> t	I <sup>2</sup> t for fusing	$V_R = 0$	14.25	MA <sup>2</sup> s

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R <sub>th(j-c)</sub>	Thermal resistance – junction to case	Double side cooled	DC	-	0.00603	.c\M
		Single side cooled	Anode DC	-	0.01024	.c\M
			Cathode DC	-	0.01467	.c/M
R <sub>th(c-h)</sub>	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	.c\M
		(with mounting compound)	Single side	-	0.002	.c/M
T <sub>vj</sub>	Virtual junction temperature	On-state (conducting)		-	135	ç
		Reverse (blocking)		-	125	ç
T <sub>stg</sub>	Storage temperature range			-55	125	°C
F <sub>m</sub>	Clamping force			74.0	91.0	kN





## **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditio	Test Conditions		Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125 ℃	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125℃		300	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125℃, ga	ite open	-	2000	V/µs
dl/dt	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub>	Repetitive 50Hz	-	400	A/μs
		Gate source 30V, 10Ω,	Non-repetitive	-	1000	A/μs
		t <sub>r</sub> < 0.5μs, T <sub>j</sub> = 125℃				
V <sub>T(TO)</sub>	Threshold voltage – Low level	1000 to 2600A at T <sub>case</sub> = 125	℃	-	0.85	V
	Threshold voltage – High level	2600 to 9000A at T <sub>case</sub> = 125	℃	-	0.99	V
r <sub>T</sub>	On-state slope resistance – Low level	1000 to 2600A at T <sub>case</sub> = 125	℃	-	0.2115	mΩ
	On-state slope resistance – High level	2600 to 9000A at T <sub>case</sub> = 125 °C		-	0.1578	mΩ
t <sub>gd</sub>	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, $10\Omega$		-	3	μs
		$t_r = 0.5 \mu s, T_j = 25 ^{\circ}\! C$				
tq	Turn-off time	$T_j = 125 ^{\circ}\text{C},$ $V_R = 200 ^{\circ}\text{V},  \text{dI/dt} = 1 ^{\circ}\text{A/}\mu\text{s},$			750	μs
		dV <sub>DR</sub> /dt = 20V/μs linear				
Qs	Stored charge	I <sub>T</sub> = 3000A, T <sub>j</sub> = 125 °C, dI/dt – 1A/μs, V <sub>Rpeak</sub> ~3100V, V <sub>R</sub> ~ 2100V		4030	5420	μC
I <sub>RR</sub>	Reverse recovery current			49	59	A
ΙL	Latching current	$T_j = 25 ^{\circ}\text{C}, \ V_D = 5 \text{V}$		-	3	Α
I <sub>H</sub>	Holding current	$T_j = 25$ °C, $R_{G-K} = \infty$ , $I_{TM} = 500$ A, $I_T = 5$ A		-	300	mA





### **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25 ℃	1.5	V
$V_{GD}$	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125 ℃	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25 ℃	300	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125 ℃	10	mA

## **CURVES**

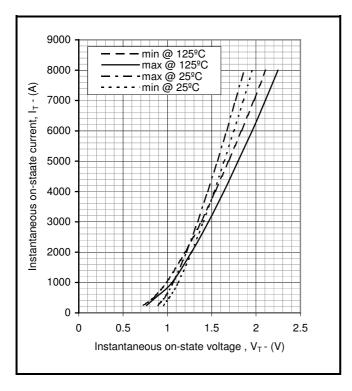


Fig.2 Maximum & minimum on-state characteristics

 $V_{\text{TM}}$  EQUATION

Where

A = 0.061592

 $V_{TM} = A + BIn(I_T) + C.I_T + D.\sqrt{I_T}$ 

B = 0.115333C = 0.000119

D = 0.002394

these values are valid for  $T_i = 125 \,^{\circ}\text{C}$  for  $I_T 250 \,^{\circ}\text{A}$  to 9000A



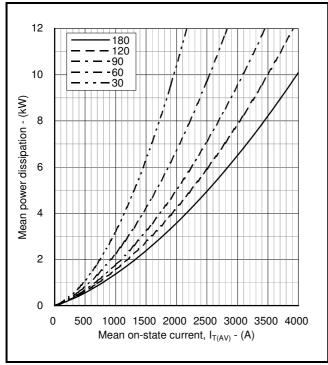


Fig.3 On-state power dissipation - sine wave

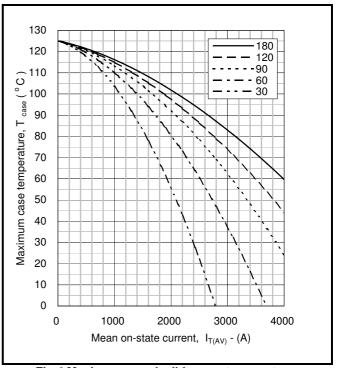


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

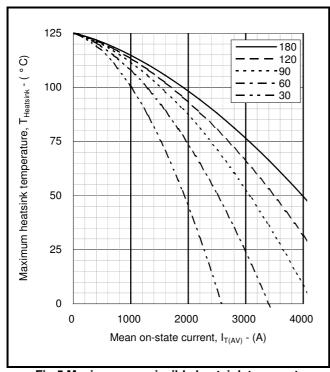


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

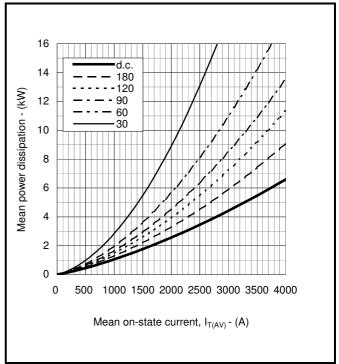


Fig.6 On-state power dissipation - rectangular wave



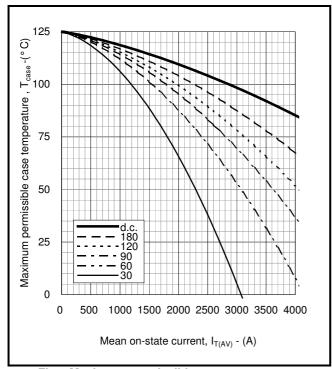


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

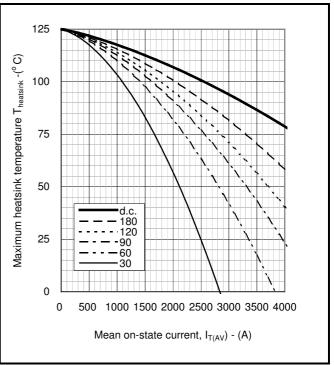
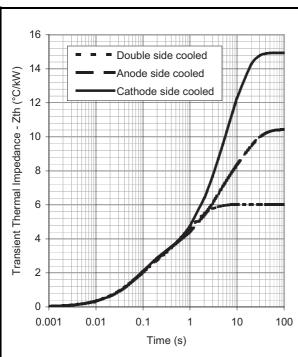


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R <sub>i</sub> (℃/kW)	3.01541	1.048955	0.983519	0.983519
Double side cooled	T <sub>i</sub> (s)	0.703874	1.904794	0.059	0.059
Anode side cooled	R <sub>i</sub> (℃/kW)	3.156003	4.092806	1.556555	1.623962
Ariode side cooled	T <sub>i</sub> (s)	2.69023	13.79162	0.059	0.205916
Cathode side cooled	R <sub>i</sub> (℃/kW)	7.077369	3.483481	1.745839	2.634274
Cathode side cooled	T; (s)	6.648601	8.436484	1.762119	0.08069

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T/T_i))]$$

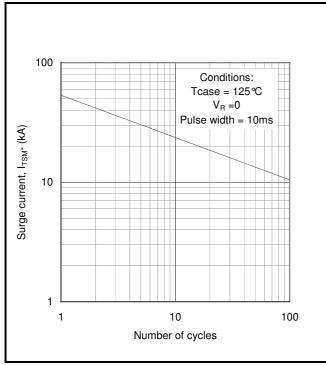
## $\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance  $R_{\text{th(j-c)}}$  when the device operates at conduction angles other than d.c.

_				_			
	ouble side c	ooling	1	Anode Side Cooling			
	$\Delta Z_{th}$ (z)				$\Delta Z_t$	<sub>h</sub> (z)	
θ°	sine.	rect.		θ°	sine.	rect.	
180	0.44	0.31		180	0.42	0.30	
120	0.49	0.43		120	0.47	0.41	
90	0.55	0.49		90	0.52	0.46	
60	0.60	0.55		60	0.57	0.52	
30	0.64	0.61		30	0.61	0.58	
15	0.66	0.64		15	0.62	0.61	

Catl	node Sided Cooling					
	ΔZ	th (z)				
θ°	sine.	rect.				
180	0.42	0.30				
120	0.47	0.41				
90	0.52	0.46				
60	0.57	0.52				
30	0.60	0.58				

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)





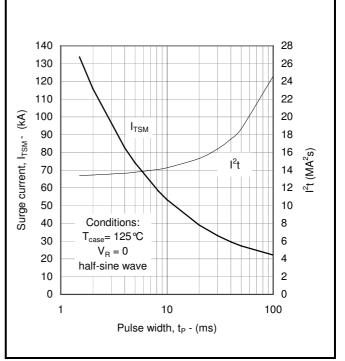


Fig.11 Single-cycle surge current

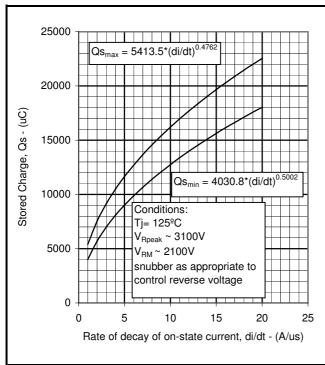


Fig.12 Stored charge

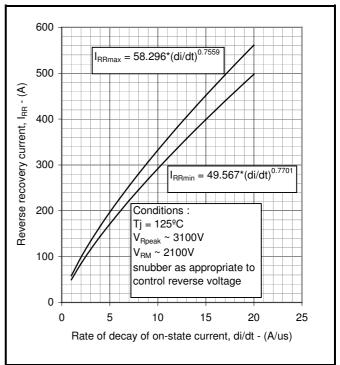


Fig.13 Reverse recovery current

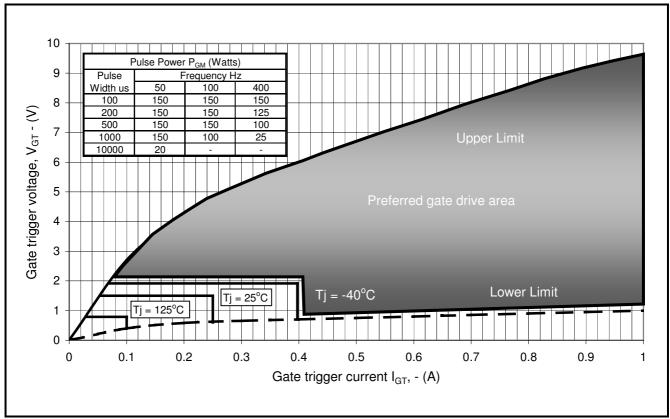


Fig14 Gate Characteristics

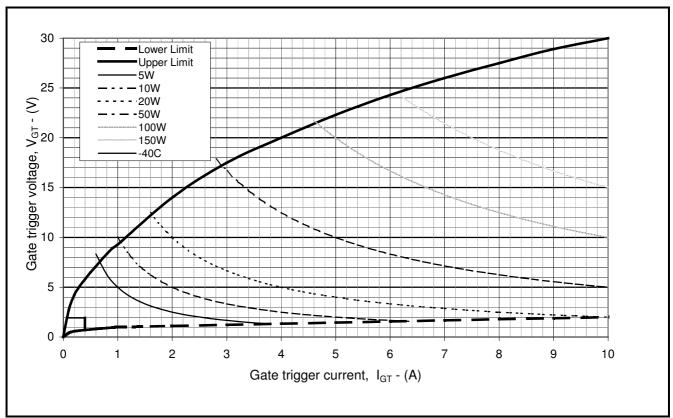


Fig. 15 Gate characteristics





#### **PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

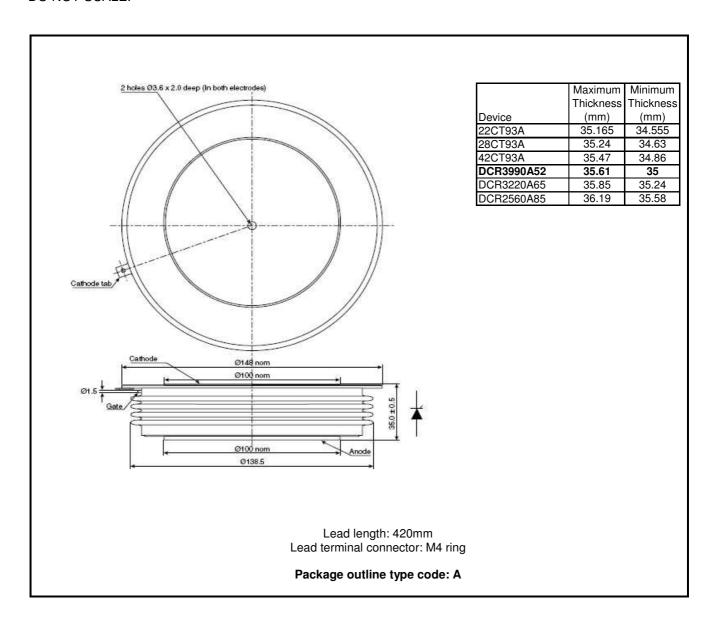


Fig.16 Package outline





#### **POWER ASSEMBLY CAPABILITY**

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

#### **HEATSINKS**

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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