



## Phase Control Thyristor

### Preliminary Information

DS5894-2 January 2010 (LN26980)

#### FEATURES

- Double Side Cooling
- High Surge Capability

#### APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

#### VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ V	Conditions
DCR470G85*	8500	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 100\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ , $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR470G80	8000	
DCR470G70	7000	

Lower voltage grades available.  
 \*8200V @  $-40^{\circ}\text{C}$ , 8500V @  $0^{\circ}\text{C}$

#### ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

#### DCR470G85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

#### KEY PARAMETERS

$V_{DRM}$	<b>8500V</b>
$I_{T(AV)}$	<b>467A</b>
$I_{TSM}$	<b>5250A</b>
$dV/dt^*$	<b>1500V/<math>\mu\text{s}</math></b>
$dI/dt$	<b>200A/<math>\mu\text{s}</math></b>

\* Higher  $dV/dt$  selections available

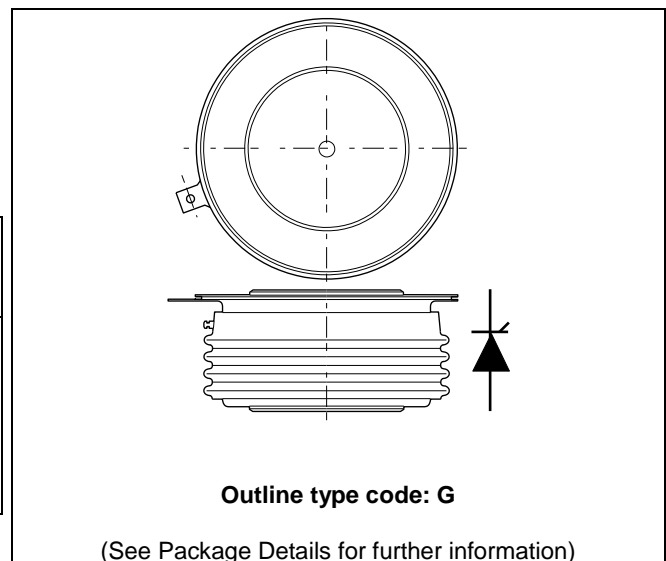


Fig. 1 Package outline

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	467	A
$I_{T(RMS)}$	RMS value	-	734	A
$I_T$	Continuous (direct) on-state current	-	725	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	5.25	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	0.138	$\text{MA}^2\text{s}$

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0268	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.0527	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0652	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 11.5kN (with mounting compound)	Double side	-	0.0072	$^{\circ}\text{C/W}$
			Single side	-	.0144	$^{\circ}\text{C/W}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}\text{C}$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}\text{C}$	
$F_m$	Clamping force		10	13	kN	

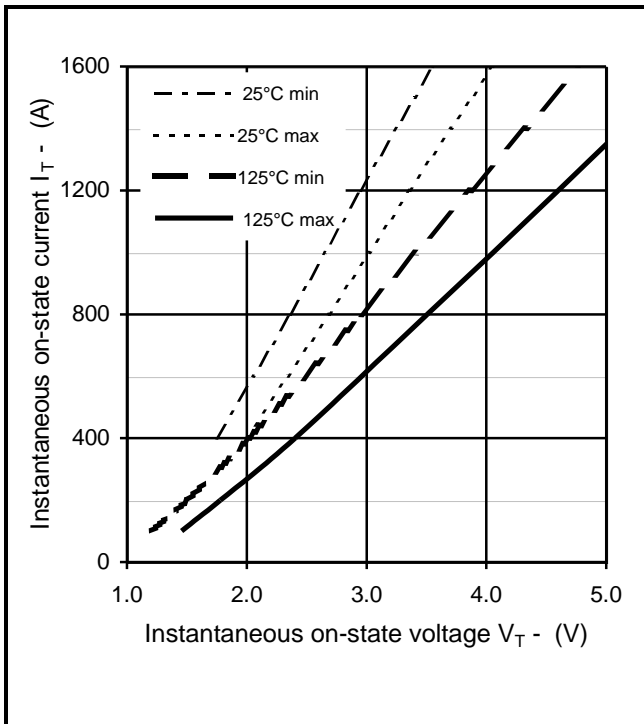
**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_{case} = 125^{\circ}C$	-	100	mA	
$dV/dt$	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^{\circ}C$ , gate open	-	1500	V/ $\mu s$	
$di/dt$	Rate of rise of on-state current	From 67% $V_{DRM}$ to $2x I_{T(AV)}$	Repetitive 50Hz	-	100	A/ $\mu s$
		Gate source 30V, 10 $\Omega$ , $t_r < 0.5\mu s$ , $T_j = 125^{\circ}C$	Non-repetitive	-	200	A/ $\mu s$
$V_{T(TO)}$	Threshold voltage – Low level	50A to 400A at $T_{case} = 125^{\circ}C$	-	1.162	V	
	Threshold voltage – High level	400A to 1600A at $T_{case} = 125^{\circ}C$	-	1.3063	V	
$r_T$	On-state slope resistance – Low level	50A to 400A at $T_{case} = 125^{\circ}C$	-	3.153	m $\Omega$	
	On-state slope resistance – High level	400A to 1600A at $T_{case} = 125^{\circ}C$	-	2.763	m $\Omega$	
$t_{gd}$	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, 10 $\Omega$ $t_r = 0.5\mu s$ , $T_j = 25^{\circ}C$	-	3	$\mu s$	
$t_q$	Turn-off time	$T_j = 125^{\circ}C$ , $V_R = 100V$ , $di/dt = 5A/\mu s$ , $dV_{DR}/dt = 20V/\mu s$ linear	-	1200	$\mu s$	
$Q_S$	Stored charge	$I_T = 500A$ , $T_j = 125^{\circ}C$ , $di/dt = 5A/\mu s$ ,	2000	3000	$\mu C$	
$I_L$	Latching current	$T_j = 25^{\circ}C$ , $V_D = 5V$	-	3	A	
$I_H$	Holding current	$T_j = 25^{\circ}C$ , $R_{G-K} = \infty$ , $I_{TM} = 500A$ , $I_T = 5A$	-	300	mA	

**GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	250	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	10	mA

**CURVES**



**Fig.2 Maximum & minimum on-state characteristics**

**V<sub>TM</sub> EQUATION**

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 1.545561  
 B = -0.202735  
 C = 0.001865  
 D = 0.066158

these values are valid for T<sub>j</sub> = 125°C for I<sub>T</sub> 50A to 1600A

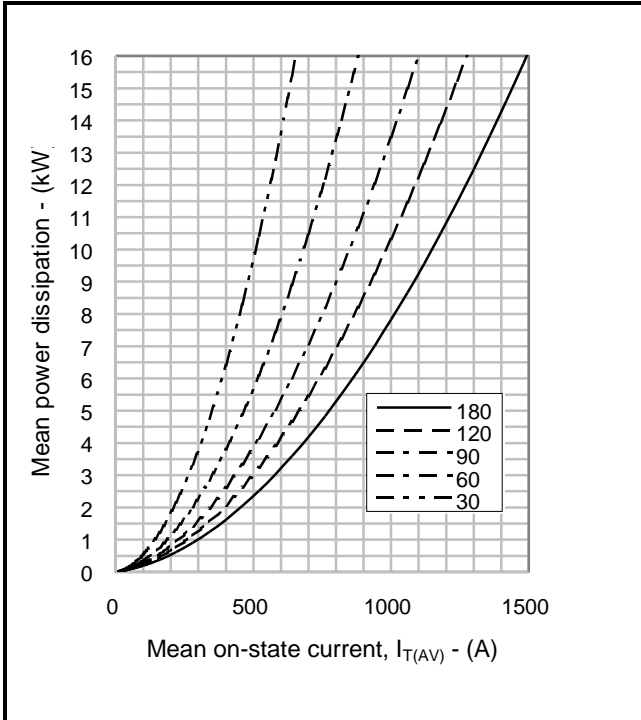


Fig.3 On-state power dissipation – sine wave

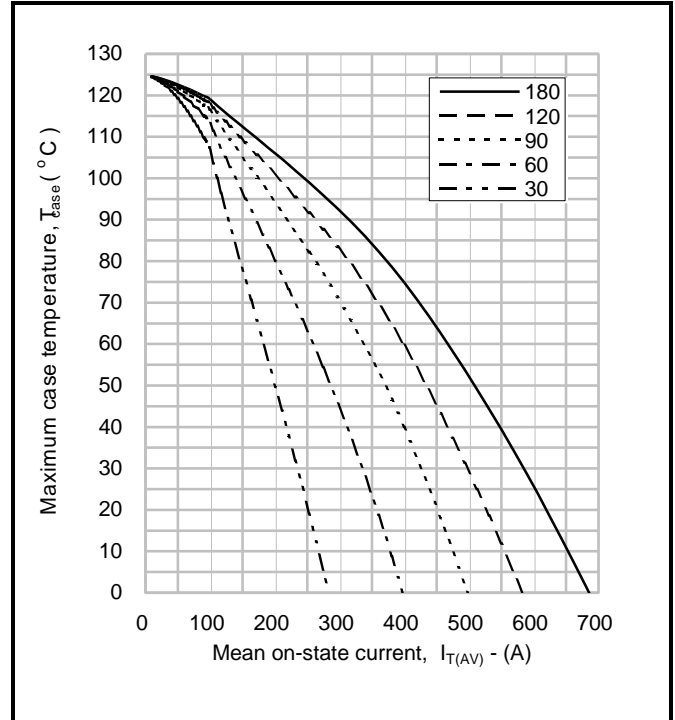


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

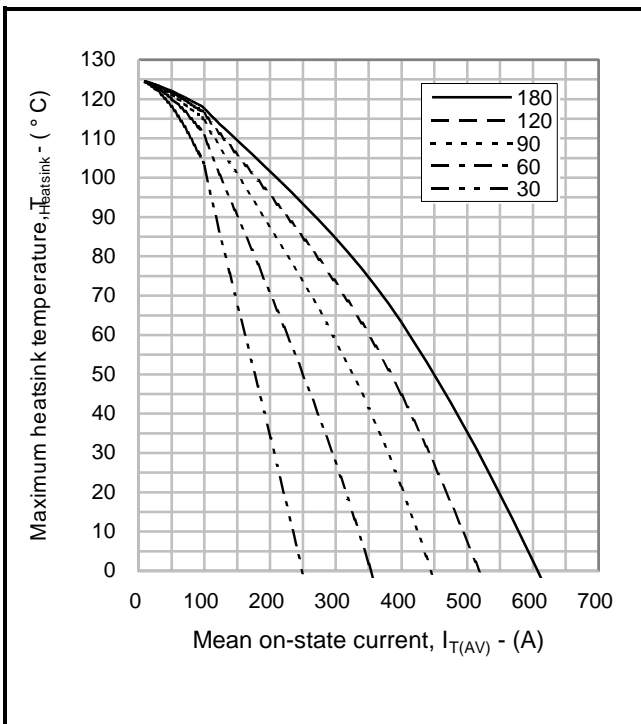


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

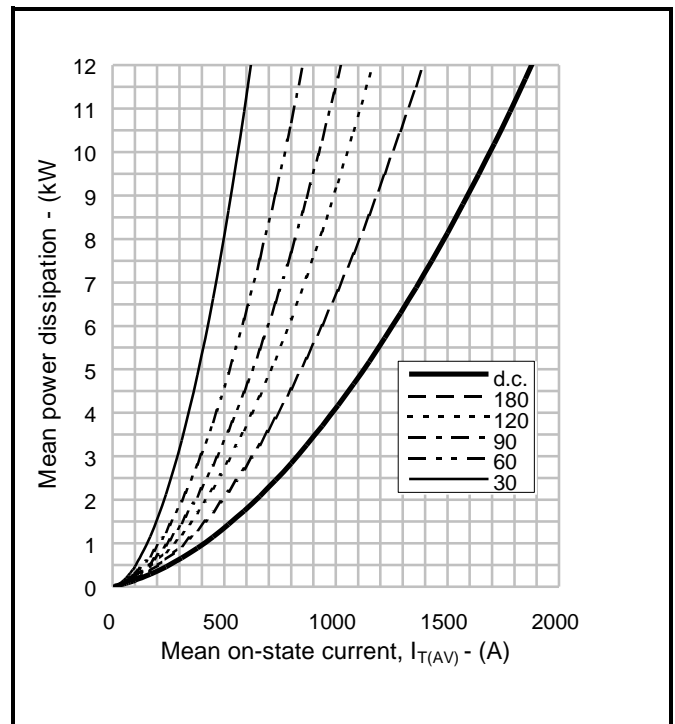
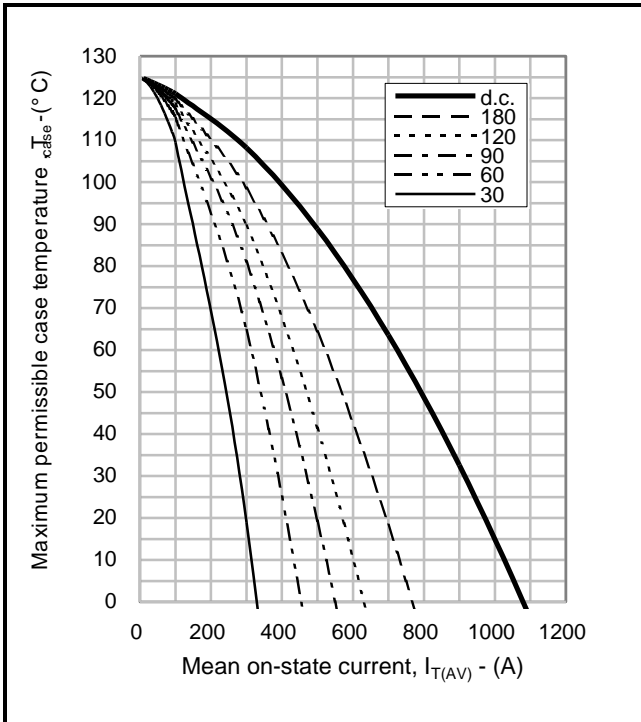
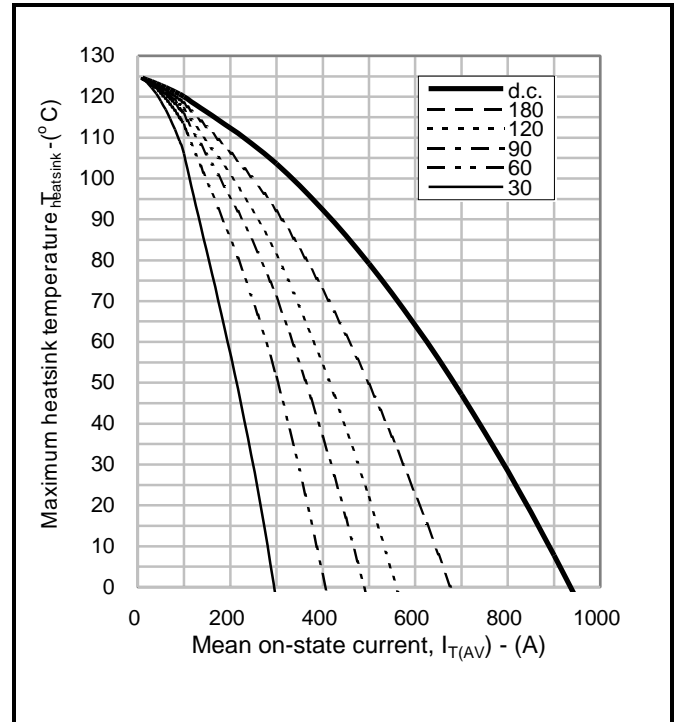


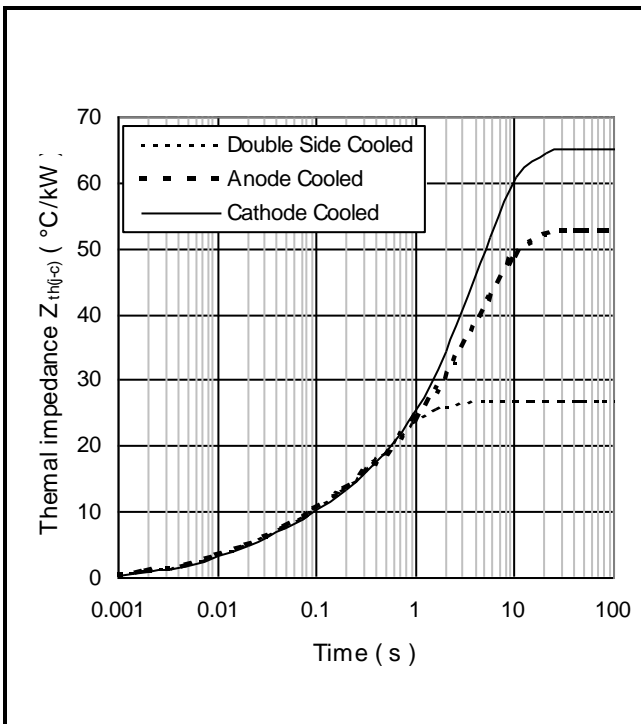
Fig.6 On-state power dissipation – rectangular wave



**Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave**



**Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave**



**Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)**

		1	2	3	4
Double side cooled	R <sub>θ</sub> (°C/kW)	2.2995	5.4226	16.9074	2.1488
	T <sub>1</sub> (s)	0.0066401	0.0457025	0.4962482	1.8248
Anode side cooled	R <sub>θ</sub> (°C/kW)	2.3214	5.2661	10.2686	34.8031
	T <sub>1</sub> (s)	0.0066948	0.045528	0.3484209	4.582
Cathode side cooled	R <sub>θ</sub> (°C/kW)	2.4895	5.9105	7.4256	49.3432
	T <sub>1</sub> (s)	0.0070404	0.052895	0.3933903	4.2295

$$Z_{th} = \sum [R_{\theta} \times (1 - \exp.(-t/t_1))] \quad [1]$$

**ΔR<sub>th(j-c)</sub> Conduction**

Tables show the increments of thermal resistance R<sub>th(j-c)</sub> when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
θ°	ΔZ <sub>th</sub> (z)		θ°	ΔZ <sub>th</sub> (z)		θ°	ΔZ <sub>th</sub> (z)	
	sine.	rect.		sine.	rect.		sine.	rect.
180	4.15	2.72	180	4.15	2.72	180	4.13	2.71
120	4.90	4.02	120	4.89	4.02	120	4.87	4.00
90	5.74	4.79	90	5.73	4.78	90	5.69	4.76
60	6.53	5.65	60	6.52	5.65	60	6.46	5.60
30	7.16	6.64	30	7.15	6.62	30	7.07	6.56
15	7.46	7.18	15	7.44	7.16	15	7.36	7.09

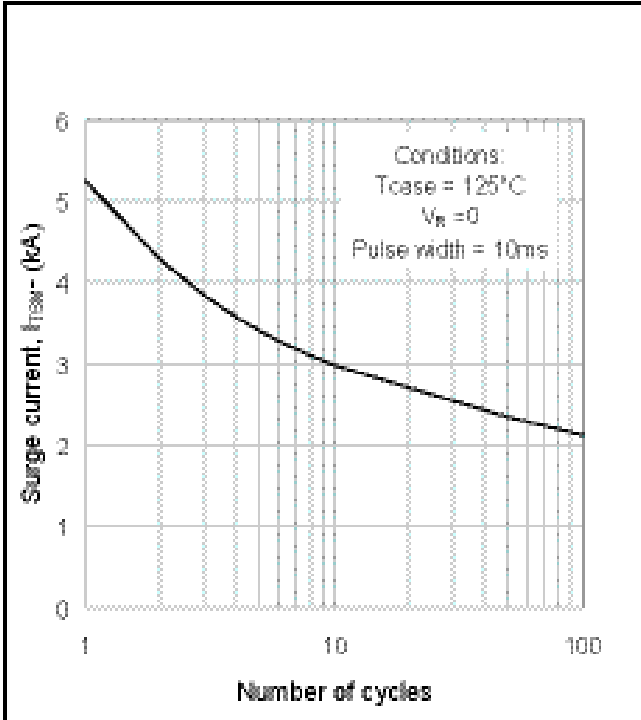


Fig.10 Multi-cycle surge current

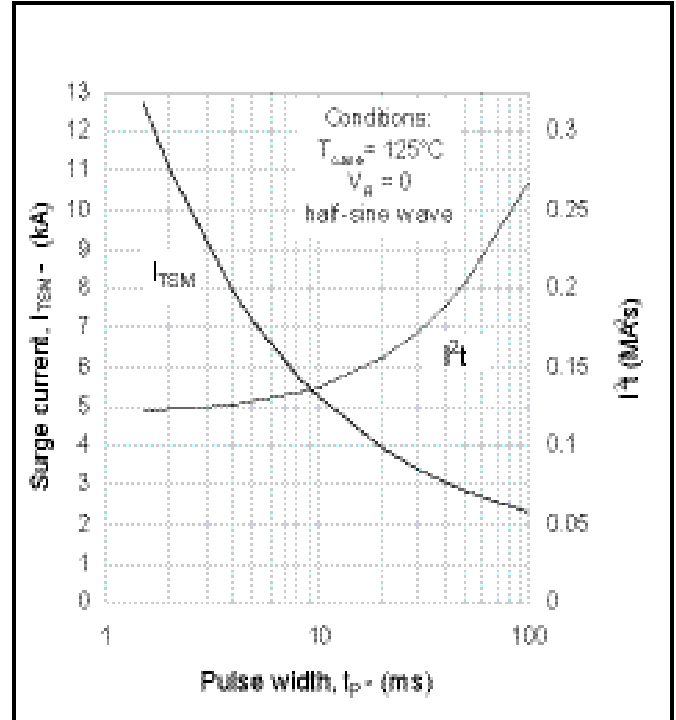


Fig.11 Single-cycle surge current

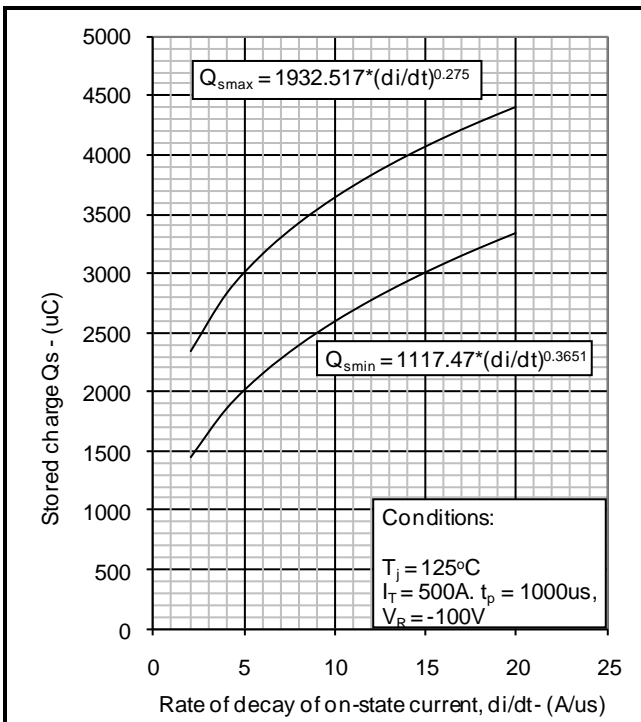


Fig.12 Stored charge

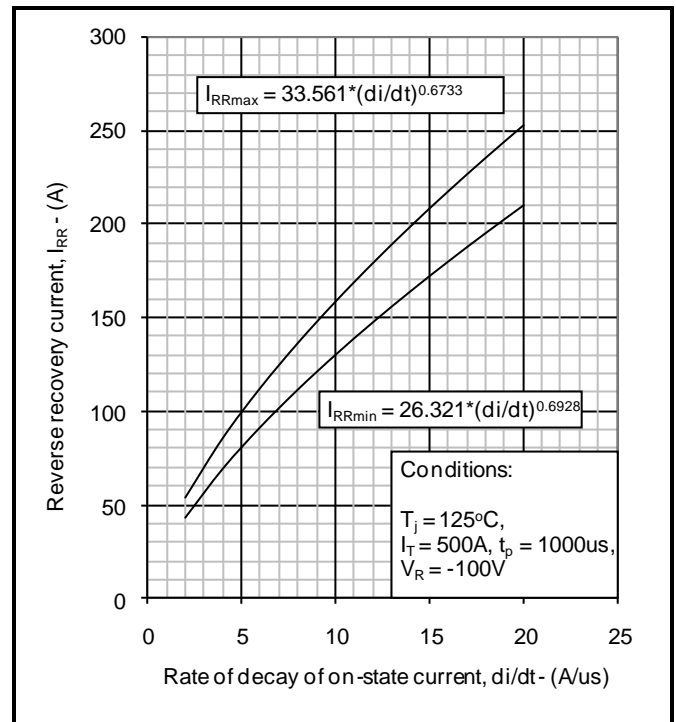


Fig.13 Reverse recovery current

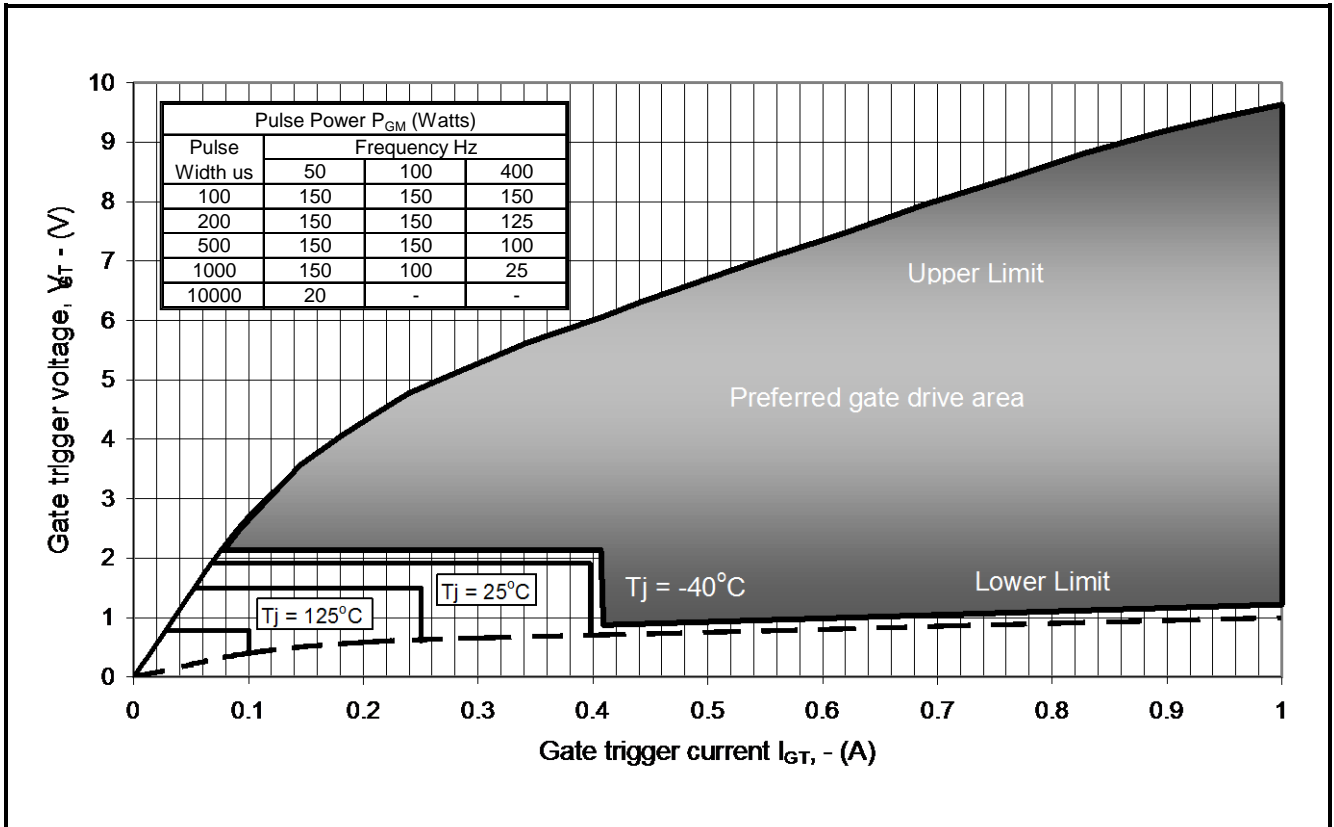


Fig14 Gate Characteristics

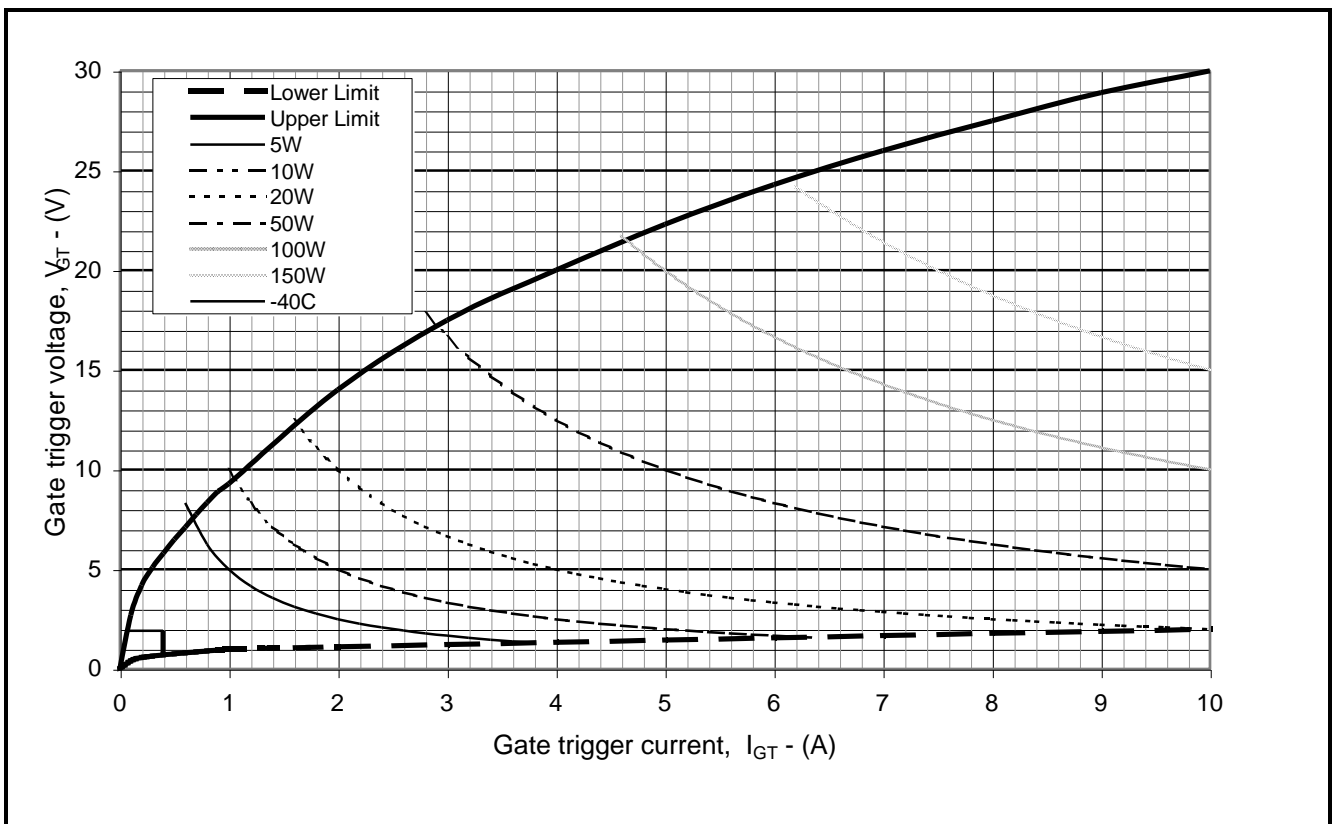
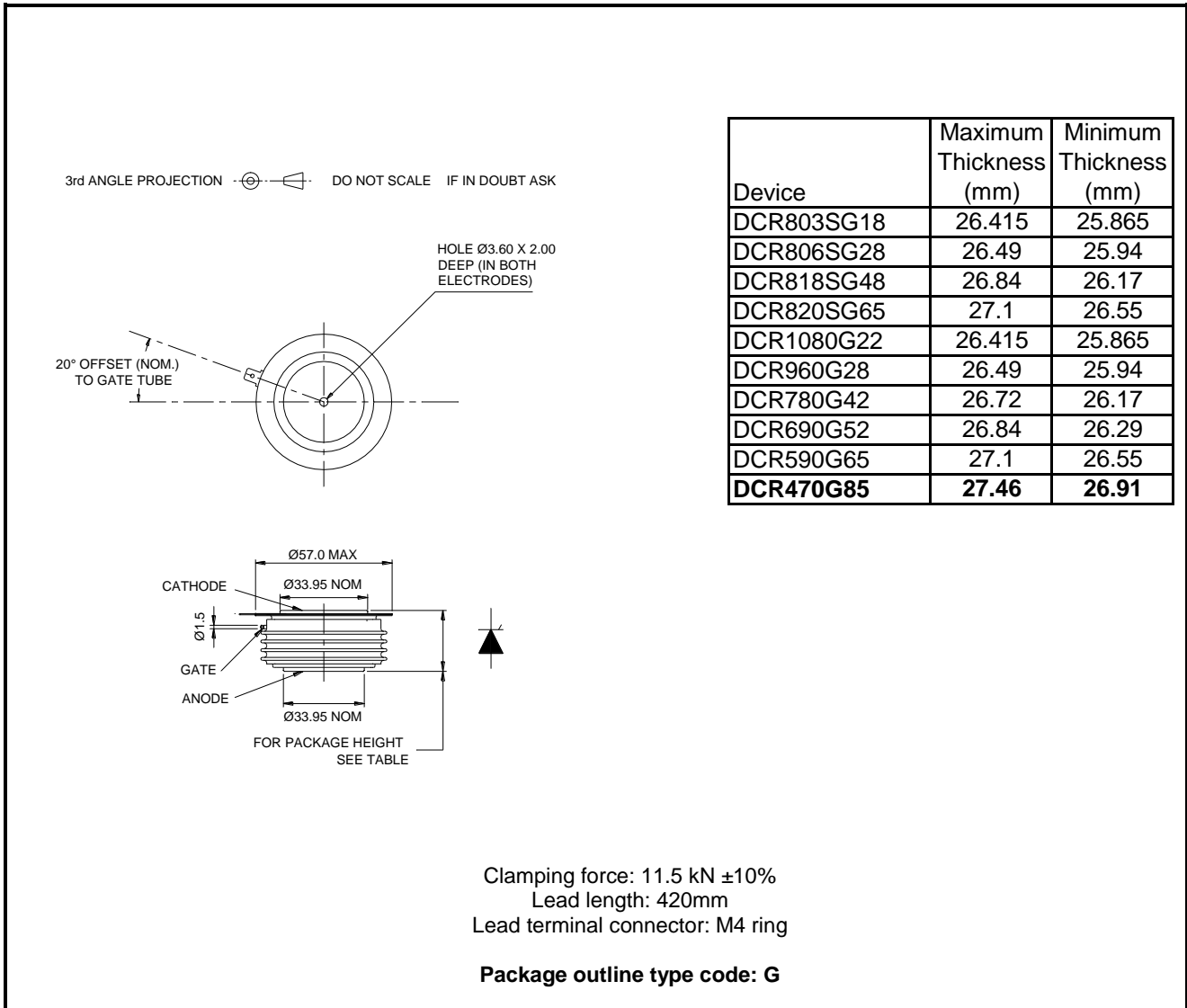


Fig. 15 Gate characteristics



**PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



**Fig.16 Package outline**

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

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