

# **DCR5980A18**

# **Phase Control Thyristor**

DS5649 1.1 January 2007 (LN25138)

### **FEATURES**

- Double Side Cooling
- High Surge Capability
- Low Inductance Internal Construction

### **APPLICATIONS**

- High Voltage Power Converters
- DC Motor Control
- High Voltage Power Supplies

#### **VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages V <sub>DRM</sub> and V <sub>RRM</sub> V	Conditions
DCR5980A18 DCR5980A16 DCR5980A14 DCR5980A12	1800 1600 1400 1200	$\begin{split} & T_{vj} = 0 \text{ C to } 125 \text{ C}, \\ & I_{DRM} = I_{RRM} = 500 \text{mA}, \\ & V_{DRM}, V_{RRM}  t_p = 10 \text{ms}, \\ & V_{DSM}  \&  V_{RSM} = \\ & V_{DRM}  \&  V_{RRM} + 100 \text{ V} \\ & \text{respectively} \end{split}$

Lower voltage grades available.

### **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

### DCR5980A14

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

#### **KEY PARAMETERS**

$V_{DRM}$	1800V
$I_{T(AV)}$	5985A
I <sub>TSM</sub>	98000A
dV/dt*	1000V/µs
dI/dt	250A/μs

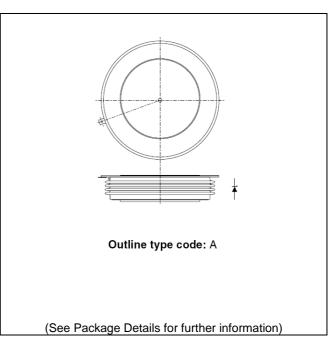


Fig. 1 Package outline



# **CURRENT RATINGS**

## $T_{case} = 60$ °C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units		
Double Si	de Cooled					
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	5985	А		
I <sub>T(RMS)</sub>	RMS value	-	9400	Α		
I <sub>T</sub>	Continuous (direct) on-state current	-	8400	Α		
Single Sid	Single Side Cooled (Anode side)					
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	3820	Α		
I <sub>T(RMS)</sub>	RMS value	-	6000	Α		
Ι <sub>Τ</sub>	Continuous (direct) on-state current	-	4920	А		

## T<sub>case</sub> = 80℃ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units			
Double Si	Double Side Cooled						
I <sub>T(AV</sub>	Mean on-state current	Half wave resistive load	4650	А			
I <sub>T(RMS)</sub>	RMS value	-	7300	А			
I <sub>T</sub>	Continuous (direct) on-state current	-	6360	А			
Single Sid	Single Side Cooled (Anode side)						
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2910	А			
I <sub>T(RMS)</sub>	RMS value	-	4570	А			
I <sub>T</sub>	Continuous (direct) on-state current	-	3630	А			



# **SURGE RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine, T <sub>case</sub> = 125°C	78.0	kA
l <sup>2</sup> t	I <sup>2</sup> t for fusing	$V_R = 50\%VRRM - \frac{1}{4}$ Sine	30.4×10 <sup>6</sup>	A <sup>2</sup> s
I <sub>TSM</sub>	Surge ( non-repetitive) on-state current	10ms half sine, T <sub>case</sub> = 125°C	98.0	kA
l <sup>2</sup> t	I <sup>2</sup> t for fusing	$V_R = 0$	48×10 <sup>6</sup>	A <sup>2</sup> s

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R <sub>th(j-c)</sub>	Thermal resistance – junction to case	Double side cooled	DC	-	0.0065	°C/W
		Single side cooled	Anode DC	-	0.013	°C/W
			Cathode DC	-	0.013	°C/W
R <sub>th(c-h)</sub>	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	°C/W
		(with mounting compound)	Single side	-	0.002	°C/W
$T_{vj}$	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T <sub>stg</sub>	Storage temperature range			-55	125	°C
F <sub>m</sub>	Clamping force			74.0	91.0	kN

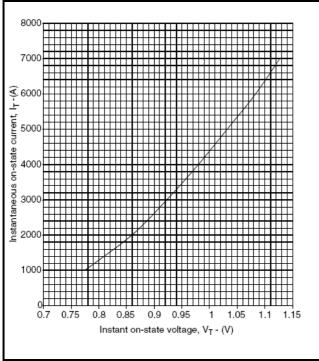


## **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		-	500	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C, ga	ate open	-	1000	V/µs
dl/dt	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 1100A	Repetitive 50Hz	-	250	A/µs
		Gate source 20V, $20\Omega$ , $t_r = 0.5 \mu s$ to 1A, $T_i = 125^\circ$	Non-repetitive	-	500	A/µs
		C				
$V_{T(TO)}$	Threshold voltage – Low level	At T <sub>vj</sub> = 125°C		-	0.77	V
r <sub>T</sub>	On-state slope resistance – Low level	At T <sub>vj</sub> = 125°C		-	0.05	mΩ
t <sub>gd</sub>	Delay time	$V_D = 67\% \ V_{DRM}, \ gate \ source \ 30V, \ 15\Omega$ $t_r = 0.5 \mu s, \ T_j = 25^{\circ} C$		1.0	1.5	μs
IL	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		150	750	mA
I <sub>H</sub>	Holding current	$T_j = 25$ °C, $V_{G-K} = \infty$		40	200	mA

## **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25℃	3.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At V <sub>DRM</sub> , T <sub>case</sub> = 125℃	0.25	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25℃	500	mA
V <sub>FGM</sub>	Peak forward gate voltage	Anode positive with respect to cathode	30	V
V <sub>FGN</sub>	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V <sub>RGM</sub>	Peak forward gate voltage	-	5	V
I <sub>FGM</sub>	Peak forward gate current	Anode positive with respect to cathode	30	А
P <sub>GM</sub>	Peak gate power	See Gate Characteristics curve/table	150	W
P <sub>G(AV)</sub>	Mean gate power	-	10	W



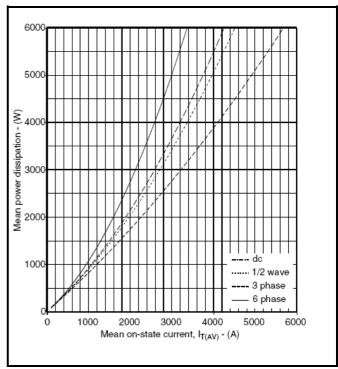


Fig.2 Maximum (limit) on-state characteristics

Fig.3 Power dissipation curves

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V_{TM} \  \, \text{Equation:-} V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T) + C.I_T + D. \\ \\ V_{TM} = A + B \text{In } (I_T)
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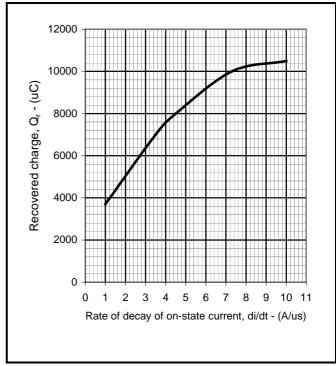


Fig.4 Recovered charge



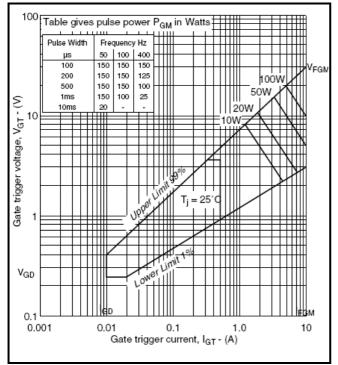


Fig.5 Gate characteristics

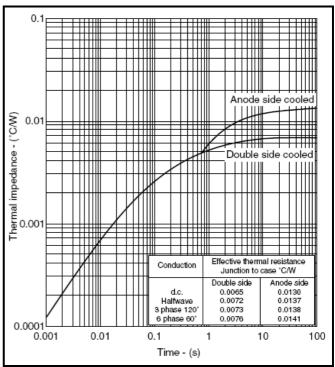


Fig.6 Maximum (limit) transient thermal impedancejunction to case (°C/W)

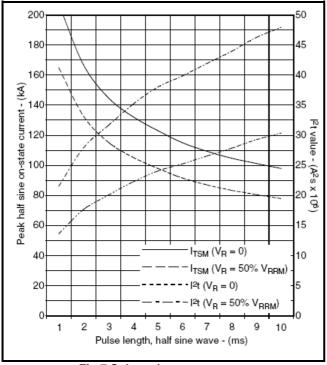


Fig.7 Sub-cycle surge current

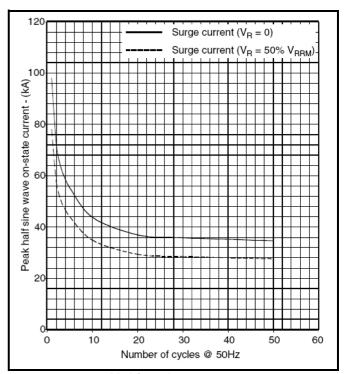


Fig.8 Multi-cycle surge current

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## **PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

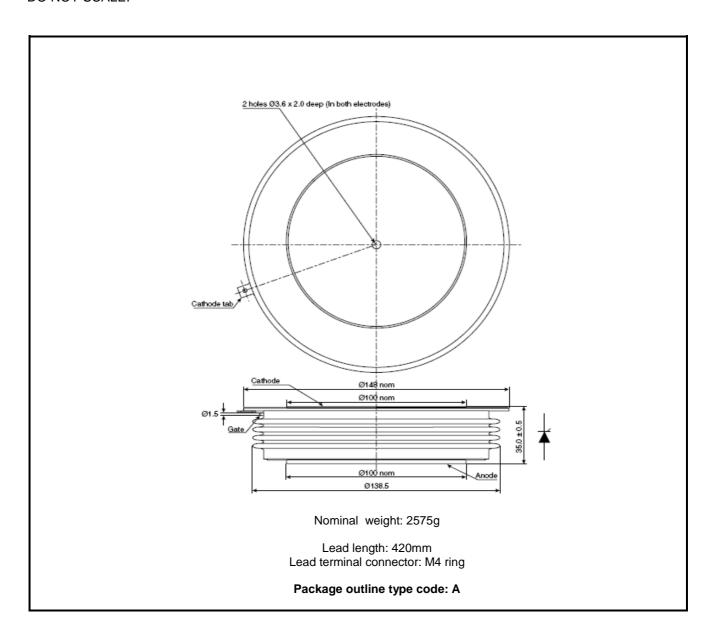


Fig.7 Package outline

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#### **POWER ASSEMBLY CAPABILITY**

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

#### **HEATSINKS**

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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