



POSEICO SPA
Power SEMiconductors Italian COrporation

POSEICO SPA
Via N. Lorenzi 8, 16152 Genova - ITALY
Tel. +39 010 6556234 - Fax +39 010 6557519
Sales Office:
Tel. +39 010 6556775 - Fax +39 010 6442510

PHASE CONTROL THYRISTOR

AT940

Repetitive voltage up to **2800 V**
Mean on-state current **4595 A**
Surge current **75 kA**

TARGET SPECIFICATION

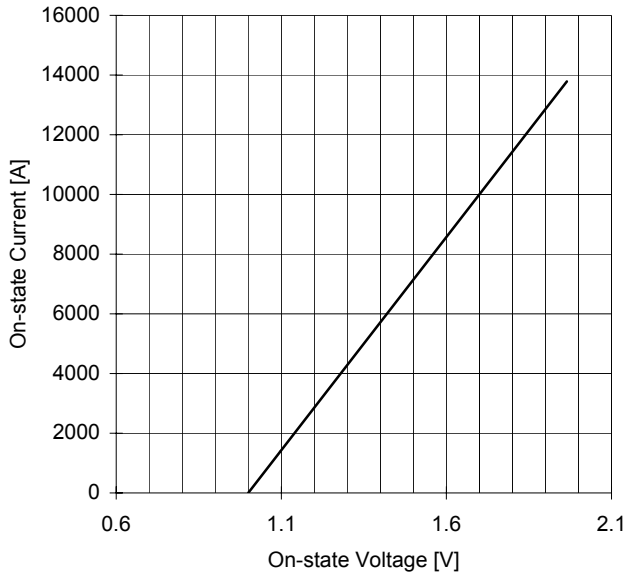
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Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM}	Repetitive peak reverse voltage		125	2800	V
V _{RSM}	Non-repetitive peak reverse voltage		125	2900	V
V _{DRM}	Repetitive peak off-state voltage		125	2800	V
I _{RRM}	Repetitive peak reverse current	V=VRRM	125	300	mA
I _{DRM}	Repetitive peak off-state current	V=VDRM	125	300	mA
CONDUCTING					
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		4595	A
I _{T(AV)}	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		3700	A
I _{TSM}	Surge on-state current	sine wave, 10 ms	125	75.0	kA
I ² t	I ² t	without reverse voltage		28125 x1E3	A ² s
V _T	On-state voltage	On-state current = 10500 A	25	1.70	V
V _{T(TO)}	Threshold voltage		125	1.00	V
r _T	On-state slope resistance		125	0.070	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM, gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	1000	V/μs
t _d	Gate controlled delay time, typical	VD=100V, gate source 10V, 10 ohm, tr=.5 μs	25		μs
t _q	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% VDRM		500	μs
Q _{rr}	Reverse recovery charge	di/dt=-20 A/μs, I= 2150 A	125		μC
I _{rr}	Peak reverse recovery current	VR= 50 V			A
I _H	Holding current, typical	VD=5V, gate open circuit	25	500	mA
I _L	Latching current, typical	VD=12V, tp=30μs	25	1000	mA
GATE					
V _{GT}	Gate trigger voltage	VD=12V	25	3.5	V
I _{GT}	Gate trigger current	VD=12V	25	400	mA
V _{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0.25	V
V _{FGM}	Peak gate voltage (forward)			10	V
I _{FGM}	Peak gate current			10	A
V _{RGM}	Peak gate voltage (reverse)			10	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μs		150	W
P _G	Average gate power dissipation			3	W
MOUNTING					
R _{th(j-h)}	Thermal impedance, DC	Junction to heatsink, double side cooled		8.5	°C/kW
R _{th(c-h)}	Thermal impedance	Case to heatsink, double side cooled		2	°C/kW
T _j	Operating junction temperature			-30 / 125	°C
F	Mounting force			80	kN
	Mass			3000	g
ORDERING INFORMATION : AT940 S 28					
standard specification <input type="checkbox"/> VDRM&VRRM/100 <input type="checkbox"/>					

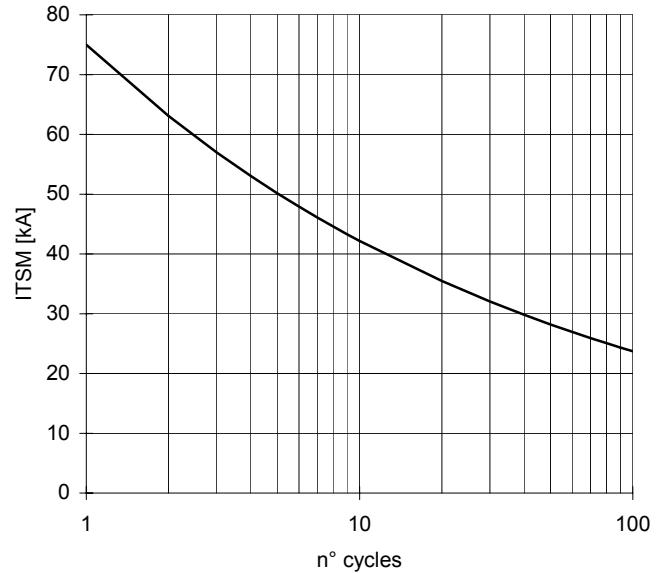
AT940 PHASE CONTROL THYRISTOR

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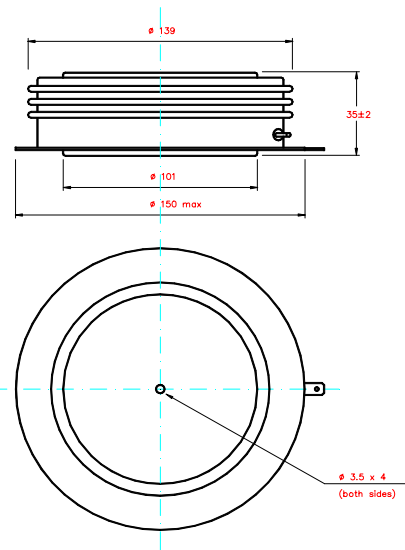
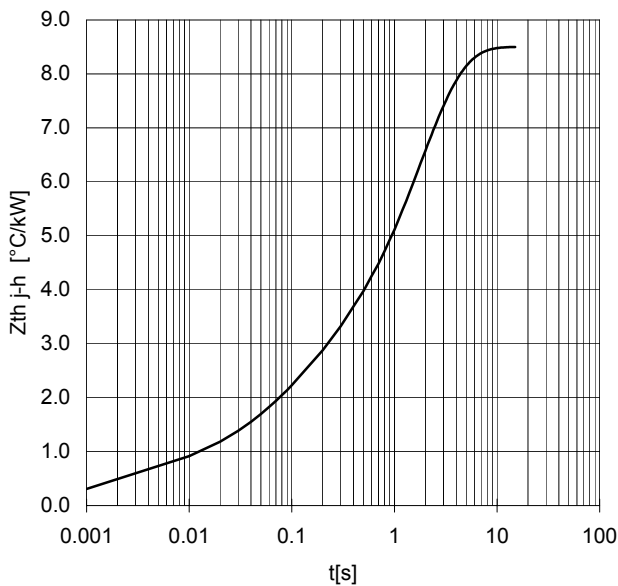
ON-STATE CHARACTERISTIC
 $T_j = 125\text{ }^\circ\text{C}$



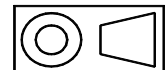
SURGE CHARACTERISTIC
 $T_j = 125\text{ }^\circ\text{C}$



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



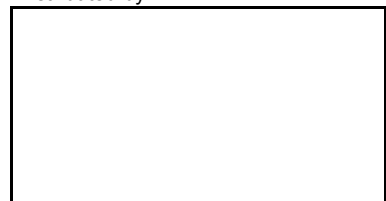
Dimensions
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

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All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm .

In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.